

LCFC Confidential

Model Name : VILE1 & VILE2
File Name : NM-A043, NM-A044
BOM P/N:

- VILE1:
- 43100108001 : SMT MB MA043 VILE1 DIS N14P 2G
 - 43100108002 : SMT MB MA043 VILE1 DIS N14M 1G
 - 43100108003 : SMT MB MA043 VILE1 UMA

- VILE2:
- 43100408001 : SMT MB MA044 VILE2 DIS N14P 2G
 - 43100408002 : SMT MB MA044 VILE2 DIS N14M 1G
 - 43100408003 : SMT MB MA044 VILE2 UMA

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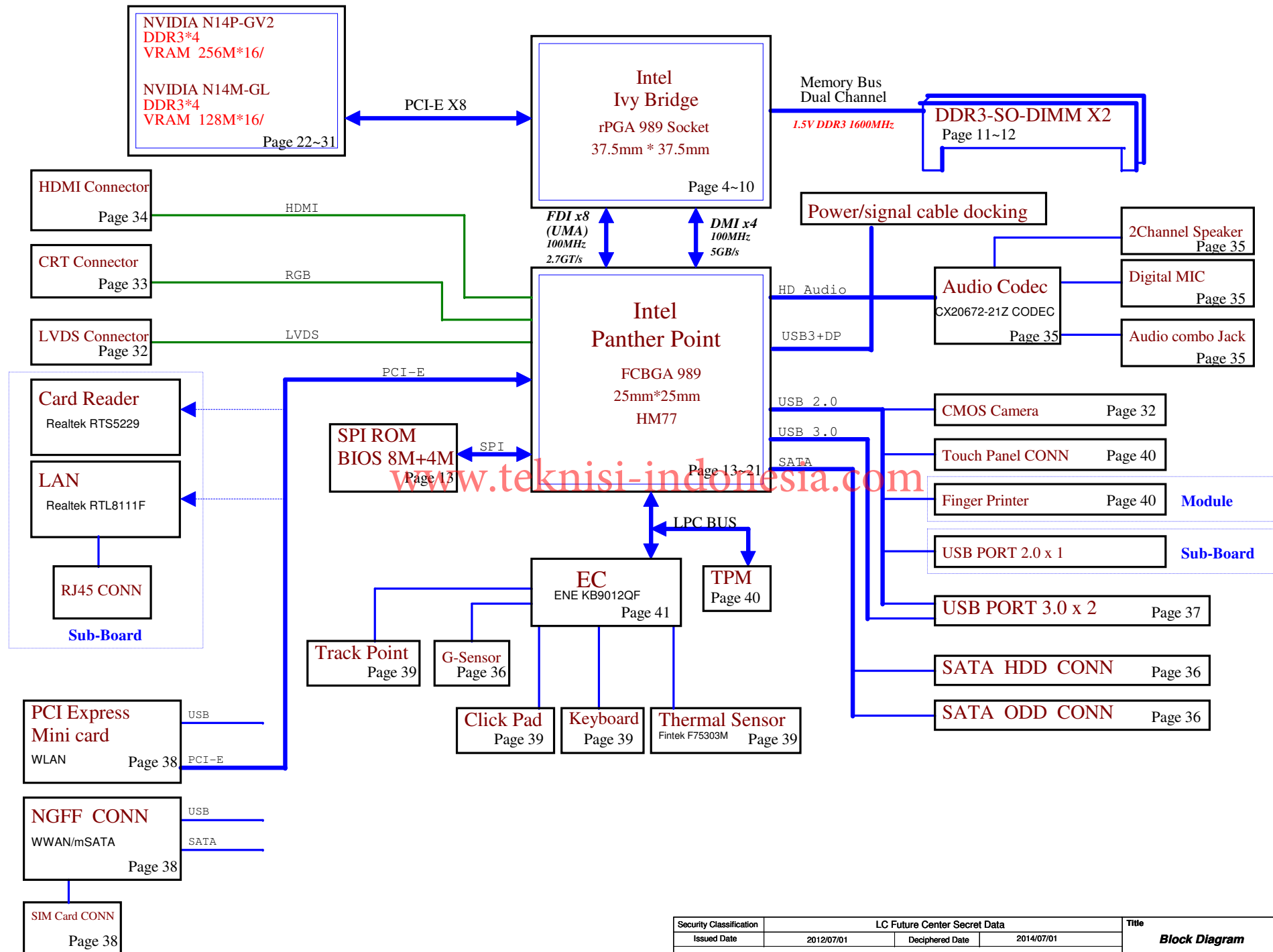
M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU hVIDIA N14M-GL / N14P-GV2

2013-04-10

REV:1.0

Model Name : VILE2



Security Classification				LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01			Block Diagram	
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Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.4
3	1.0
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M1001_101xb	

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB 2.0	UHCI0	0	USB 3.0 Port (Left Side)
		1	
	UHCI1	2	USB 3.0 Port (Left Side)
	UHCI2	3	USB 3.0 Port
	UHCI2	4	Touch Panel
EHCI2		5	
	UHCI3	6	
		7	
	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Camera

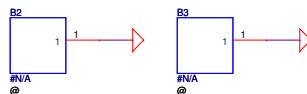
BOM Structure Table

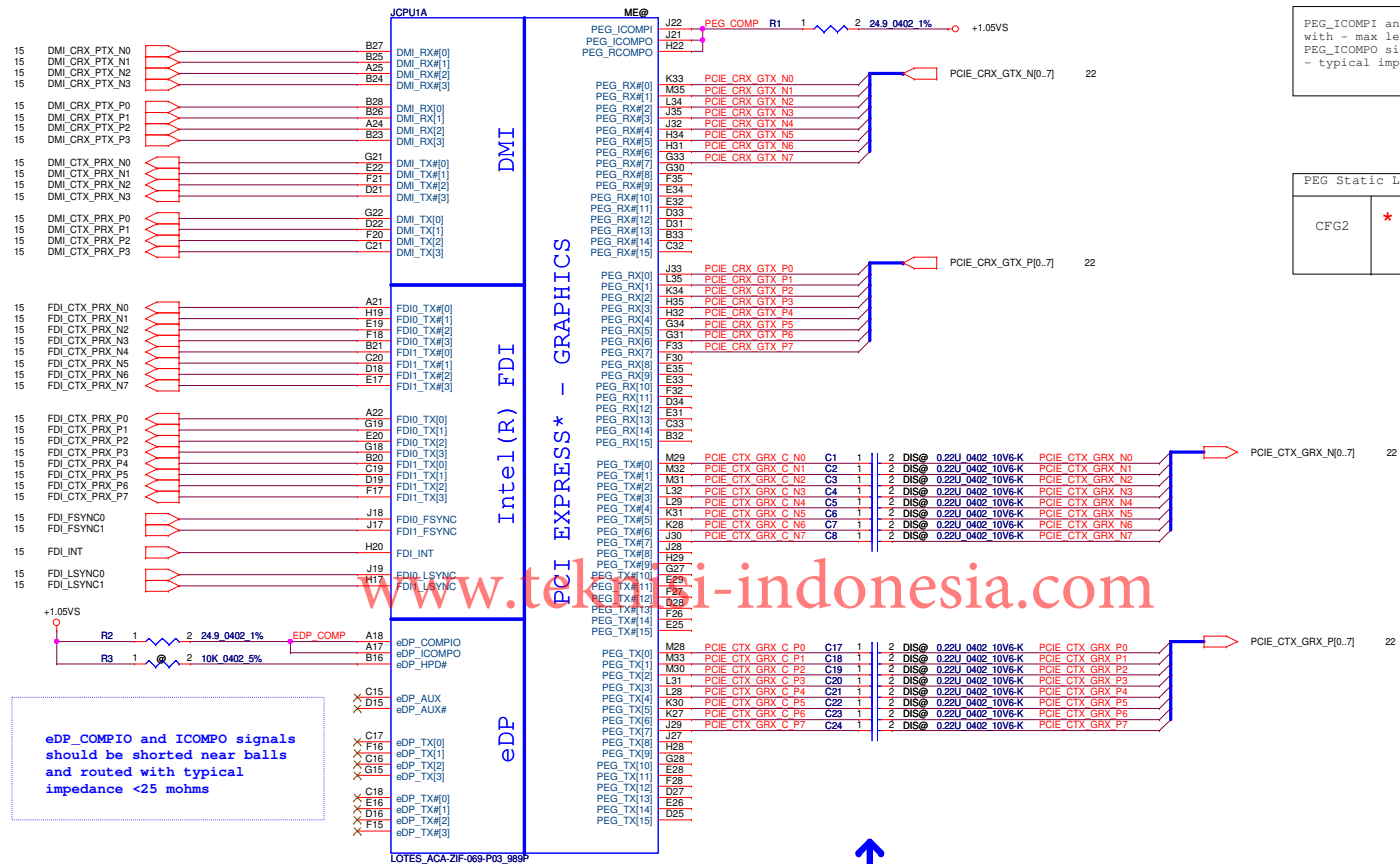
BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
Nvidia	DIS@
PCH AUX Power	+3V_PCH@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N14M-GL	N14MGL@
GPU N14P-GV2	N14PGV2@
SIM Card Slot	3G@
Touch Panel	Touch@
Finger Print Board	FP@

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	✓	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	✓	✓	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SMLOCLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	✓	X	✓	X	X	✓	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

ZZZ
NM-A044
DA80000TH10
NM-A044

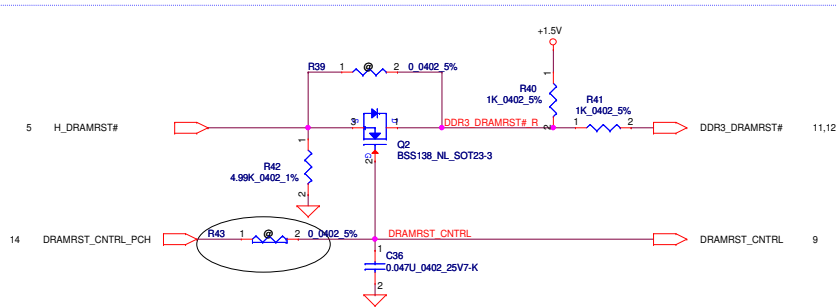
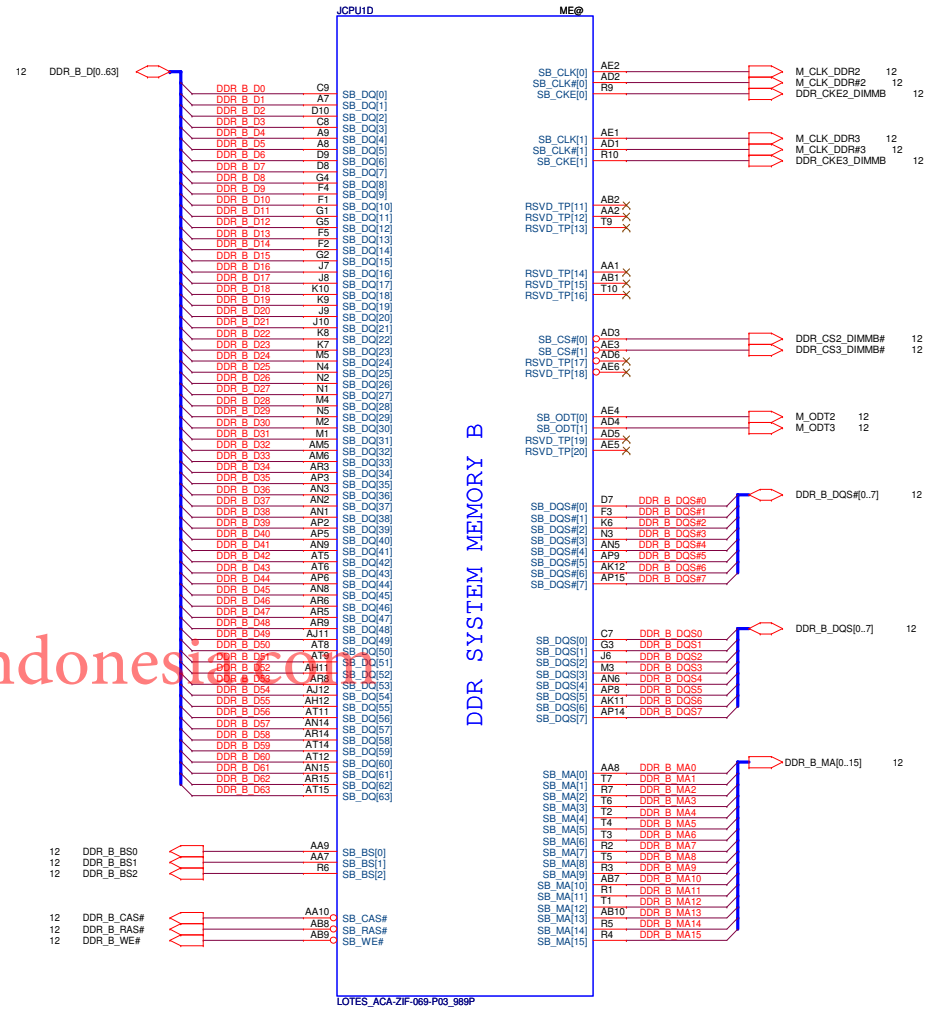
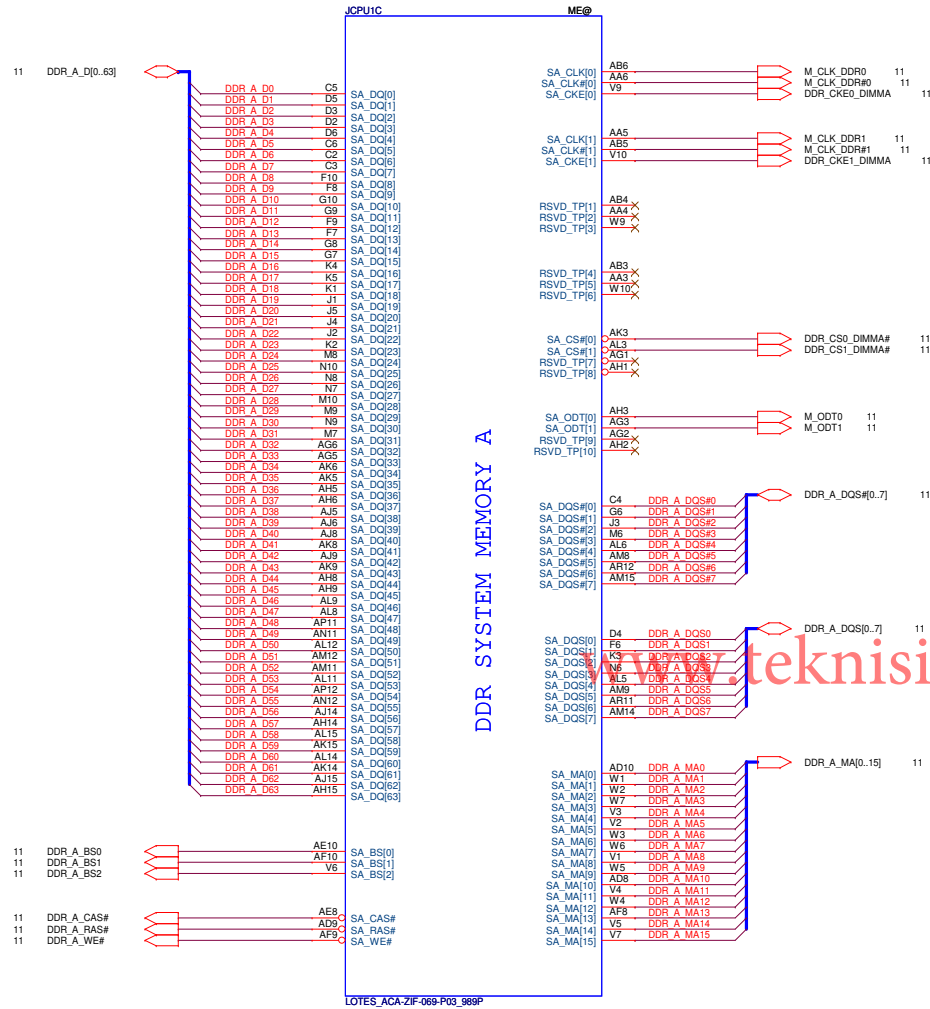




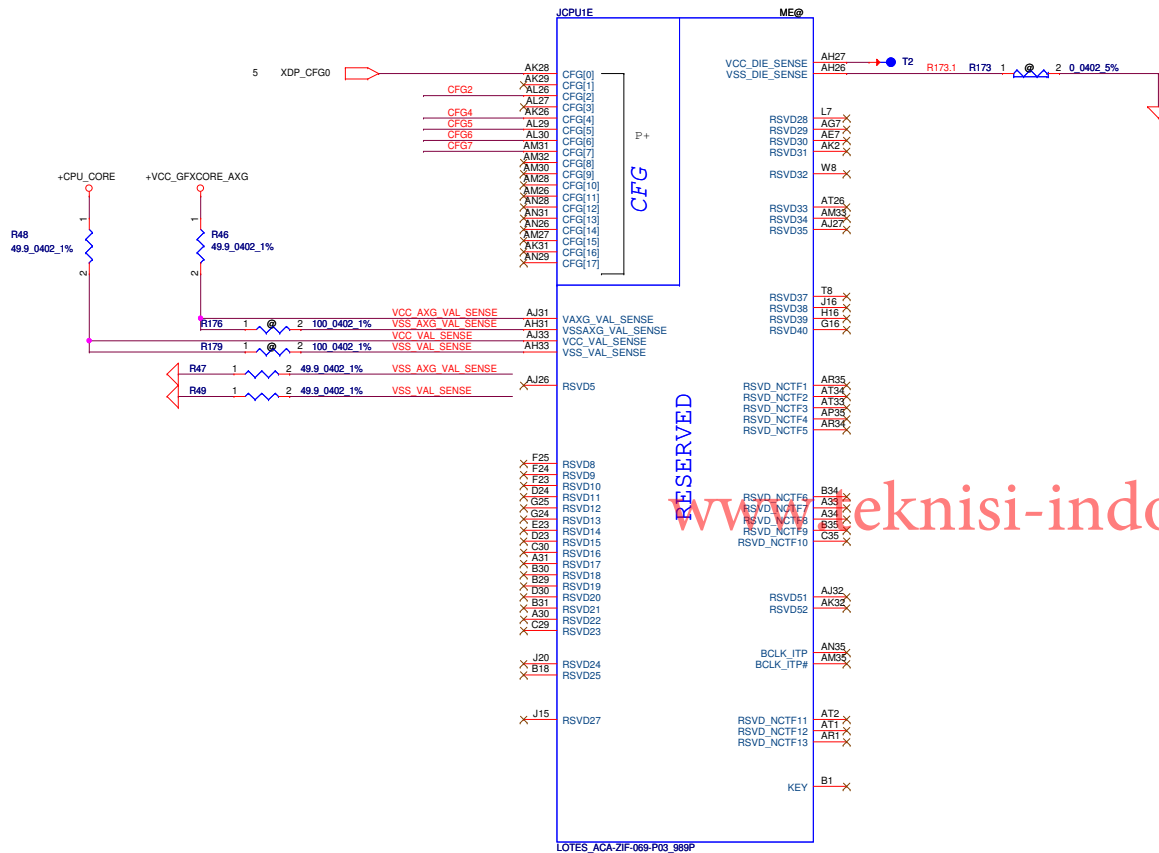
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x

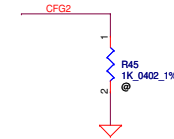
Nvidia support PCIe Gen2



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Issued Date	2012/07/01	Deciphered Date	2014/07/01			PROCESSOR(3/7) DDRIII	
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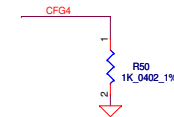


CFG Straps for Processor



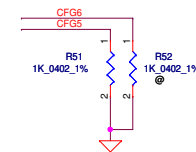
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
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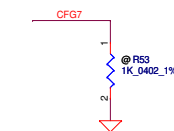
Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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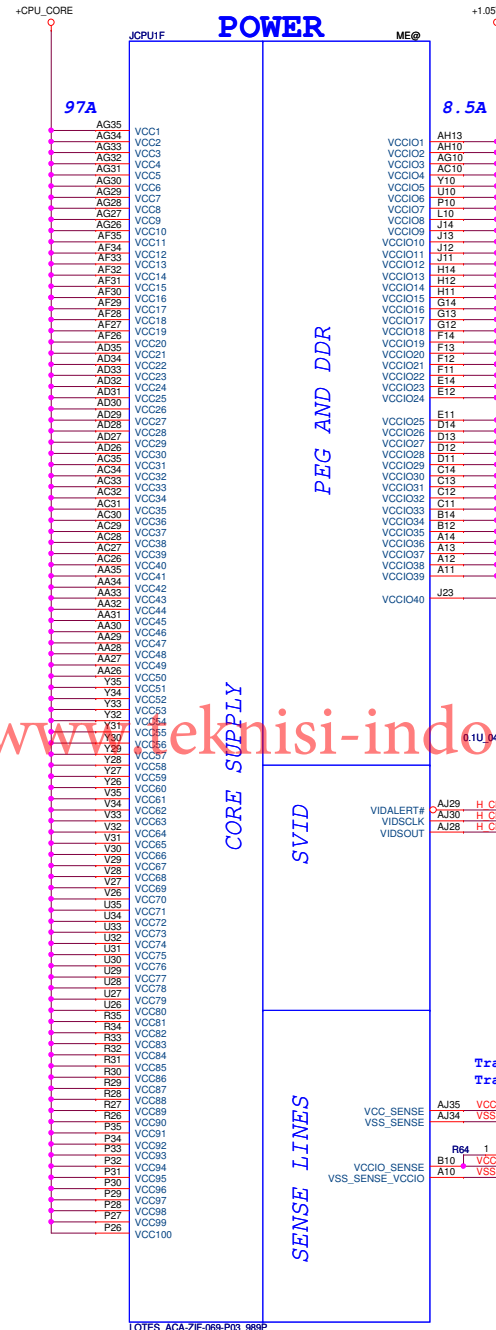
PCIe Port Bifurcation Straps

CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>
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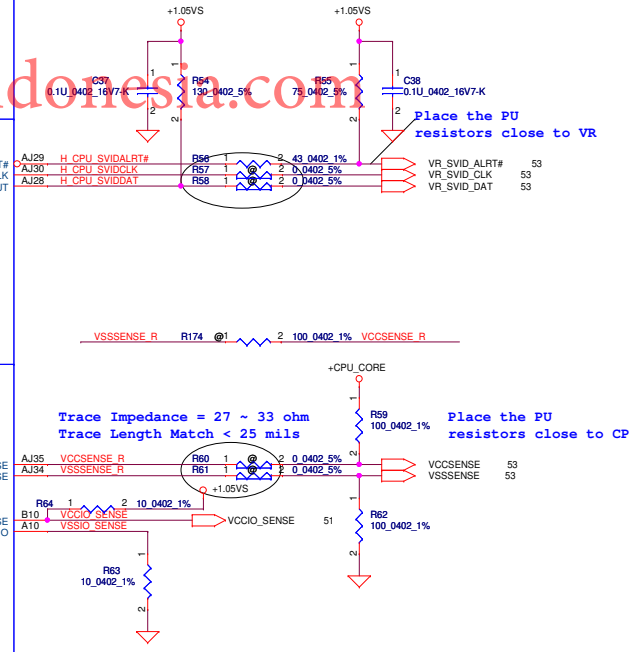


PEG DEFER TRAINING

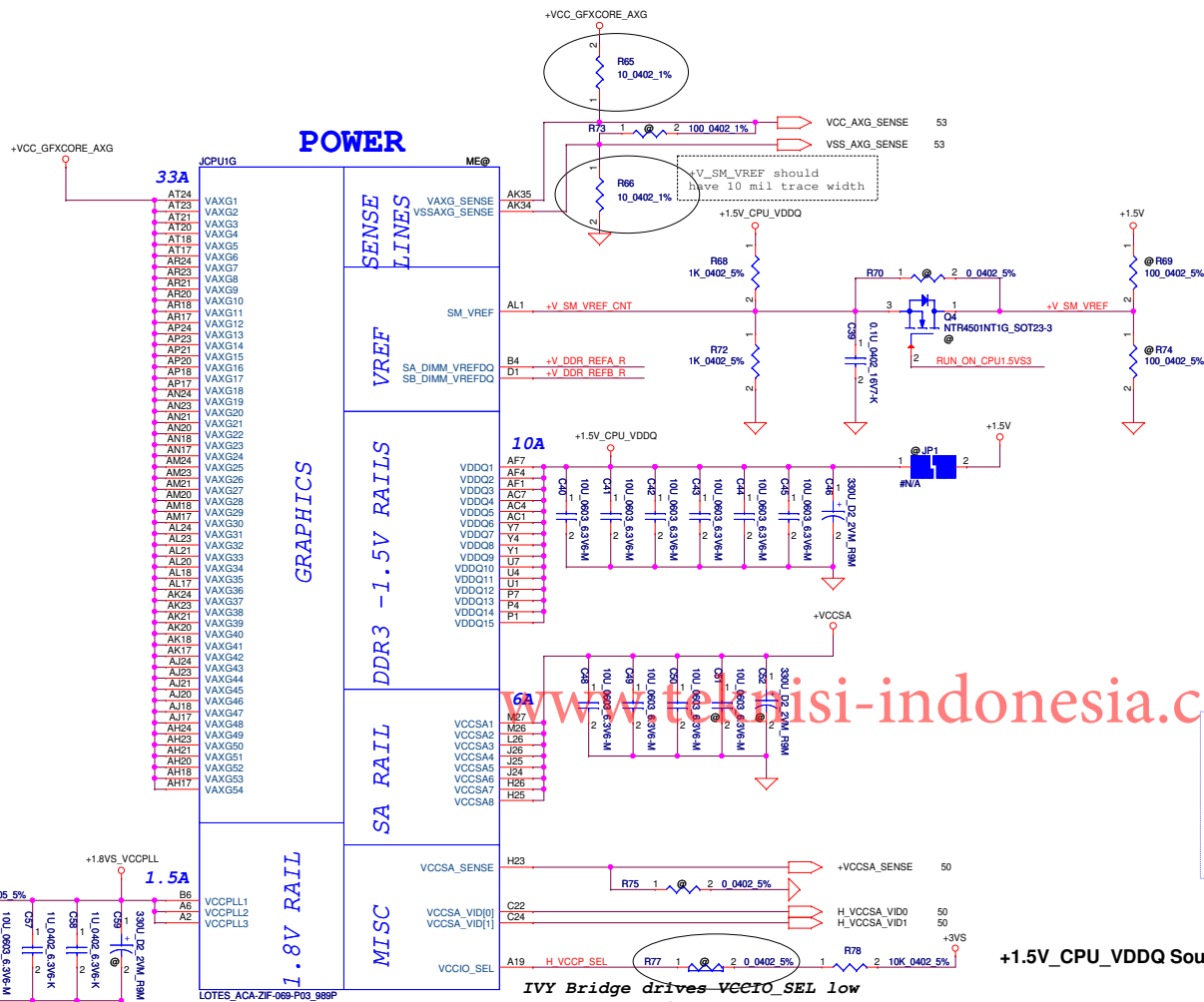
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
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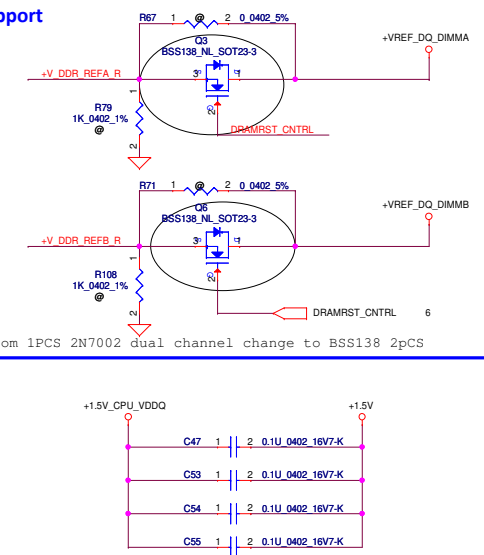
LOTES_ACA-ZIF-069-P03_969P



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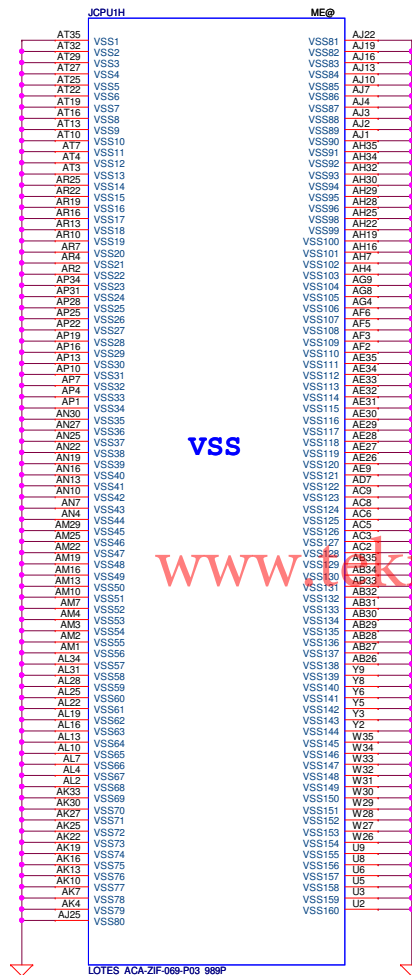
M3 Support

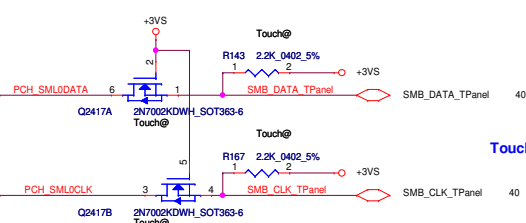
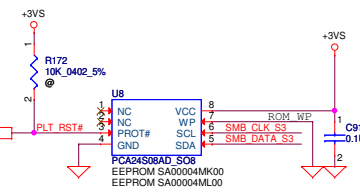
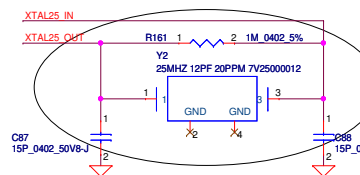
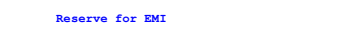
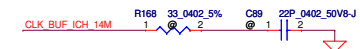
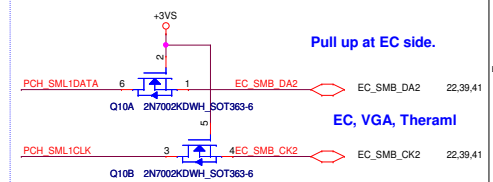
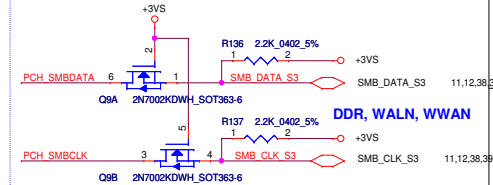
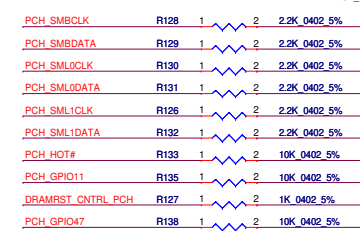
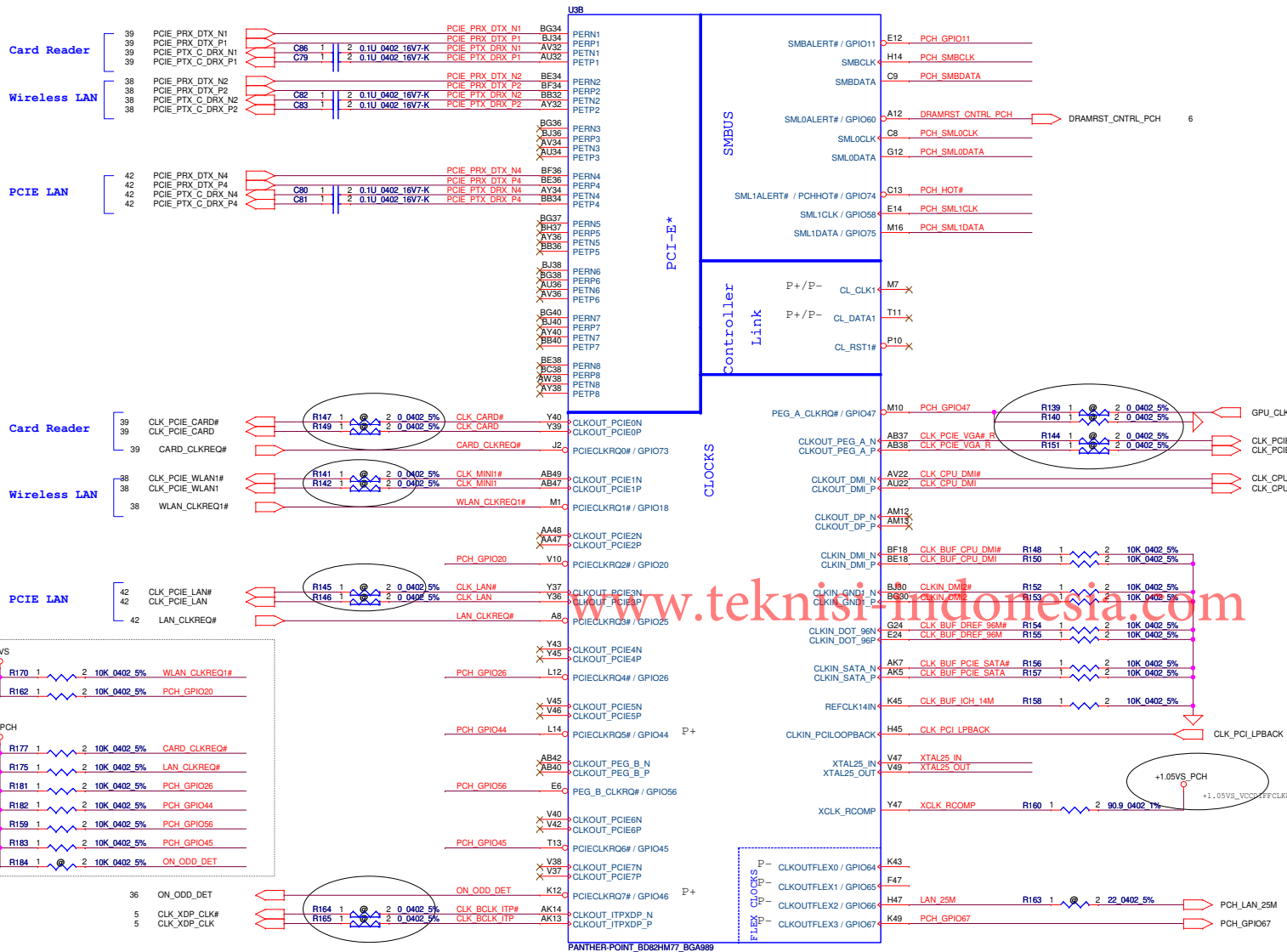



Vaxg

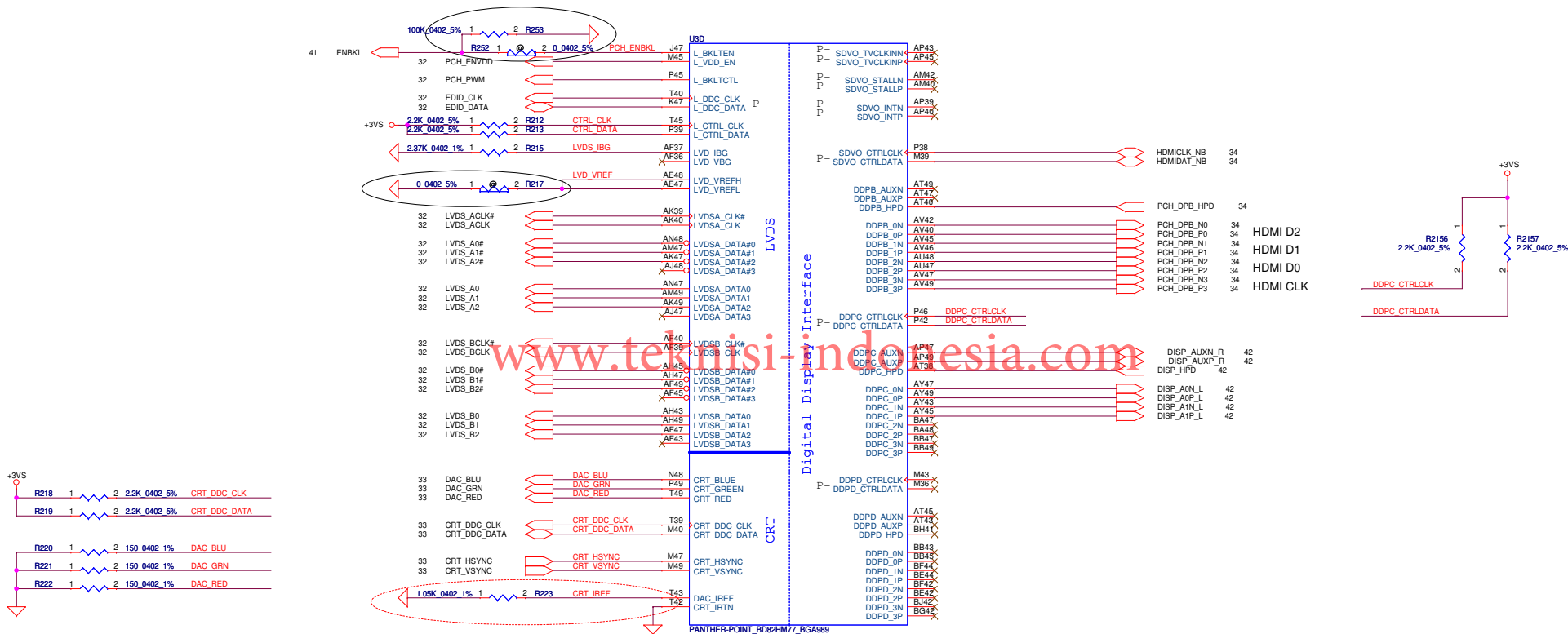
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

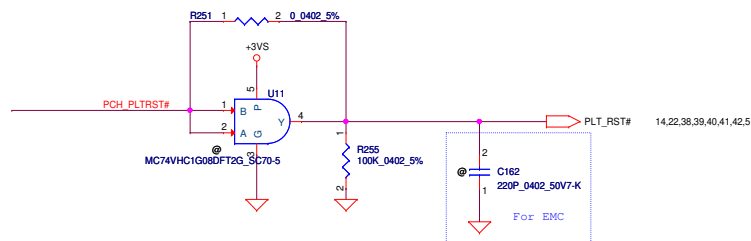
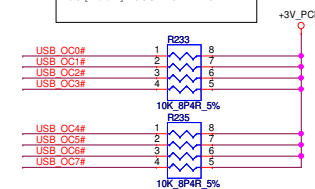
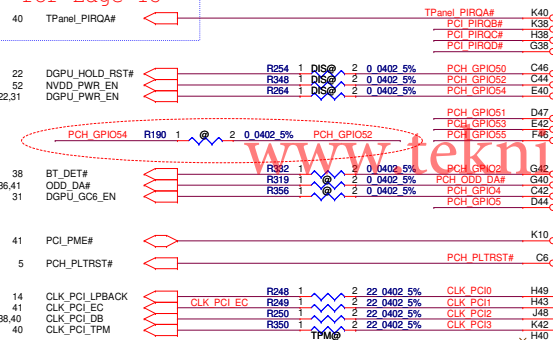
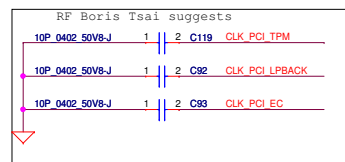
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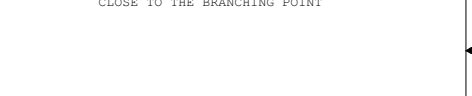
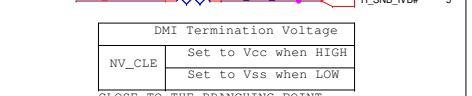
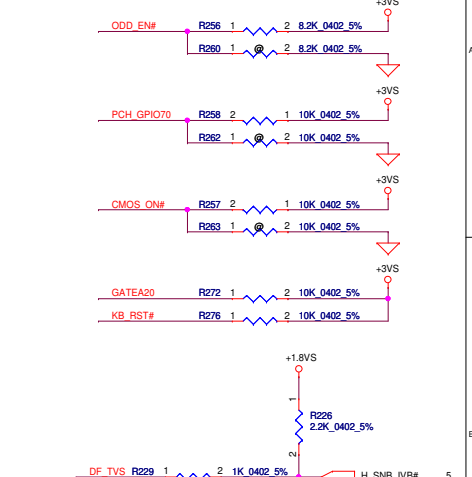
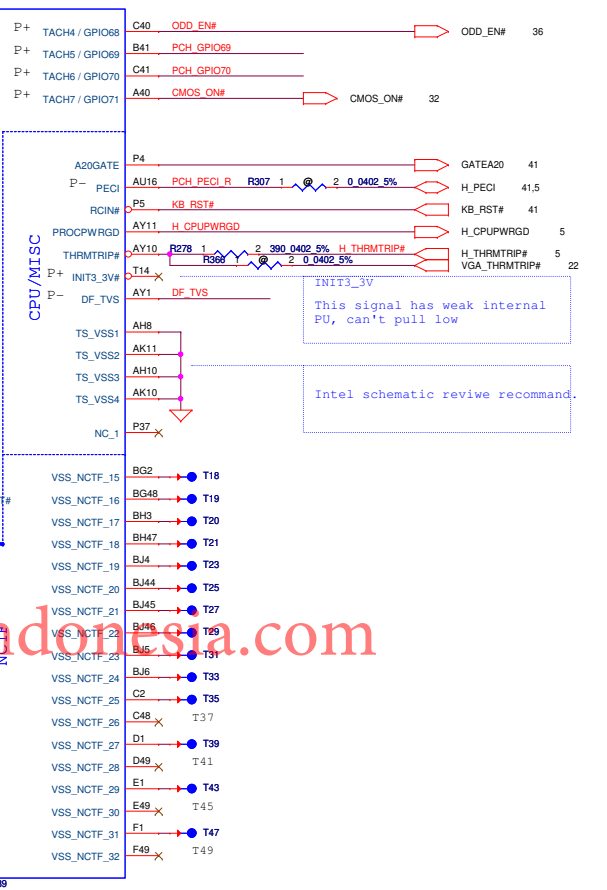
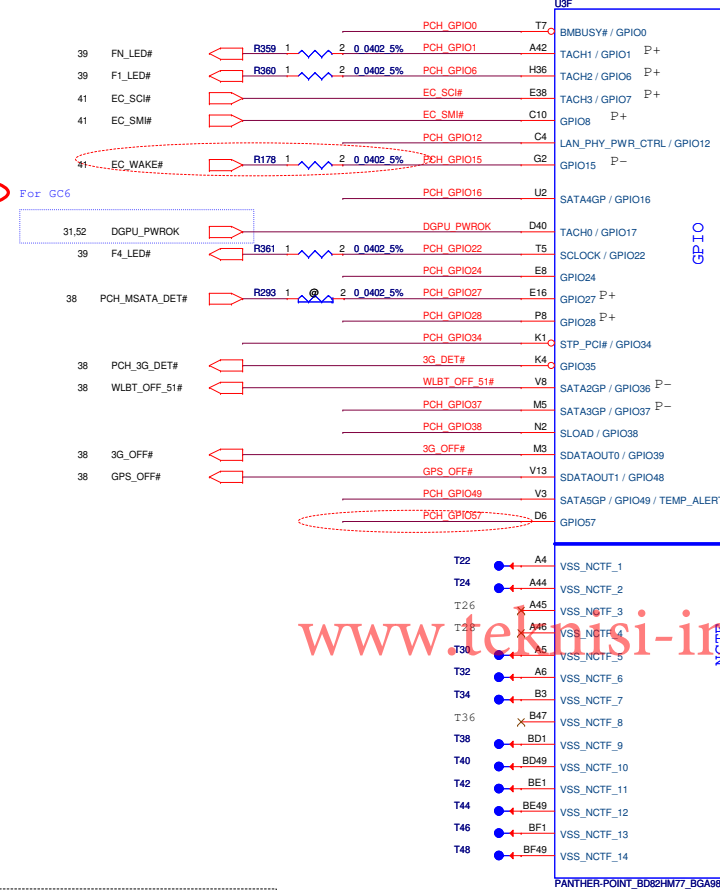
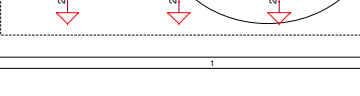
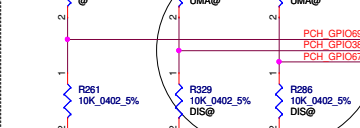
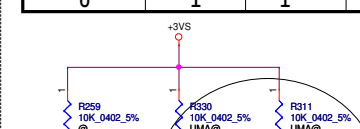
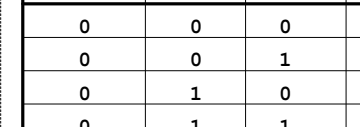
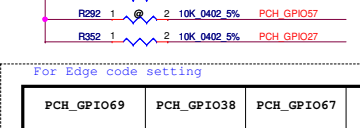
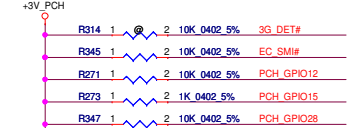
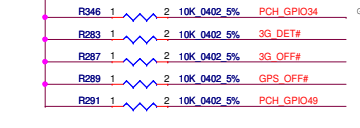
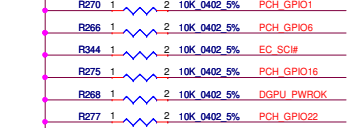
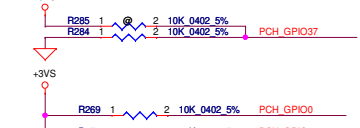
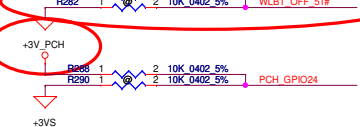
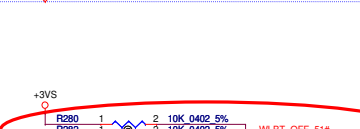
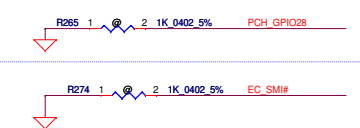
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCH (2/9) PCIE, SMBUS, CLK		
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Custom				1A		
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCH (5/9) PCI, USB, NVRAM	
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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

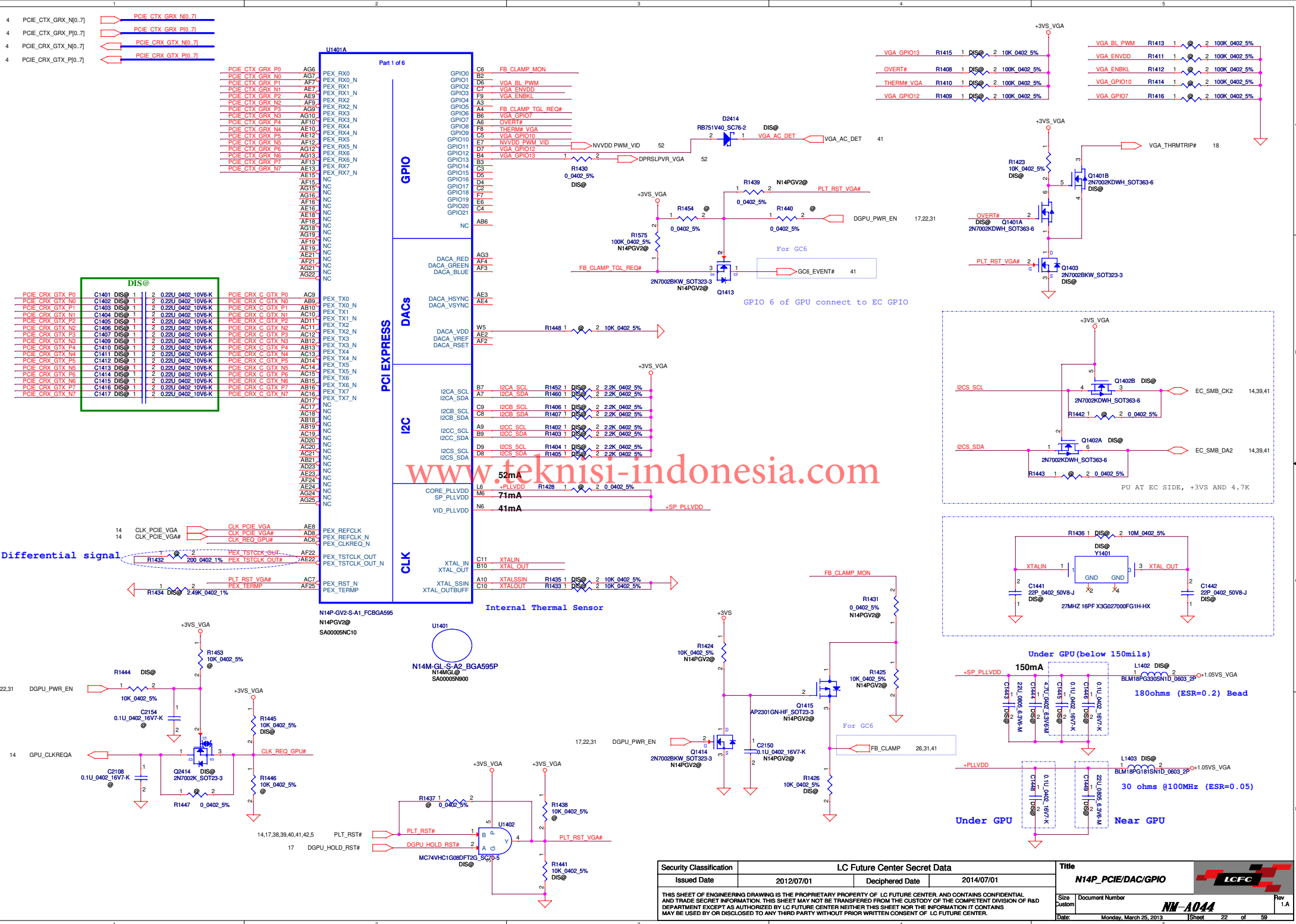


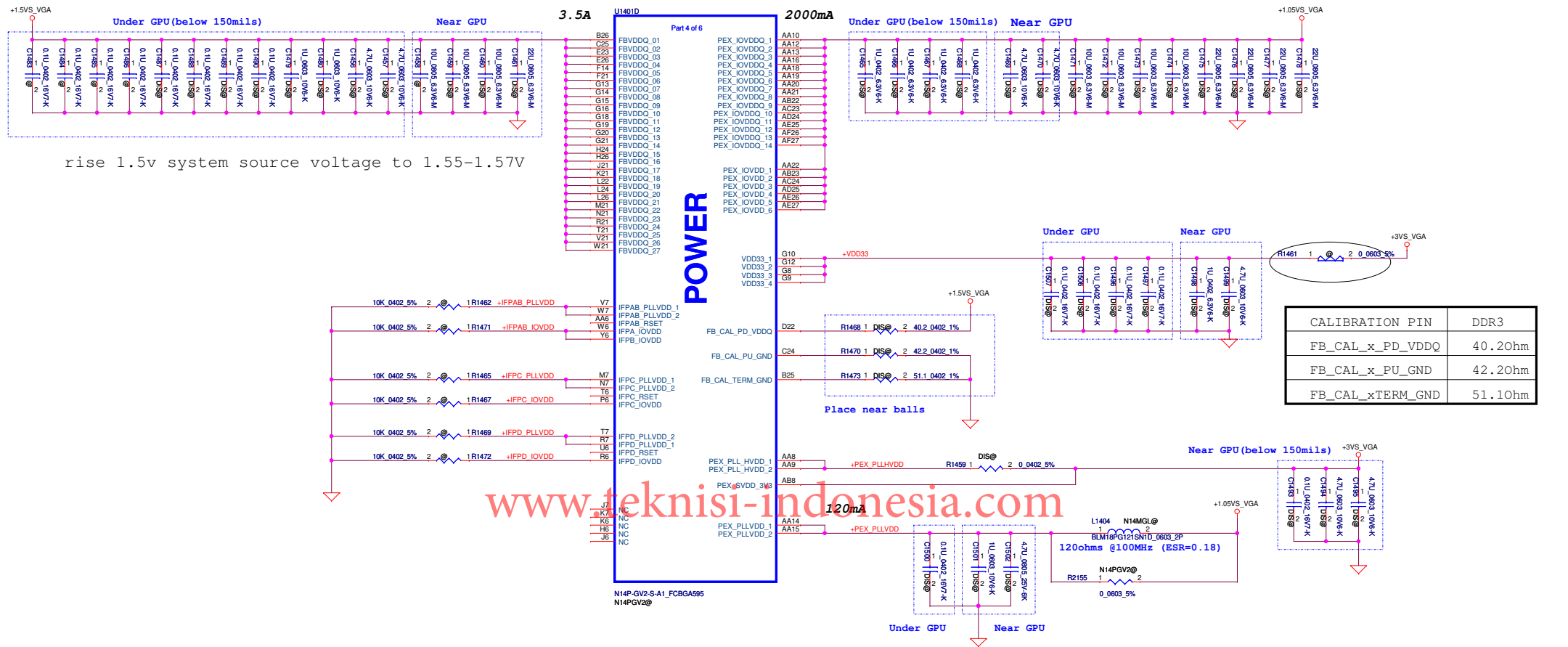
For Edge code setting

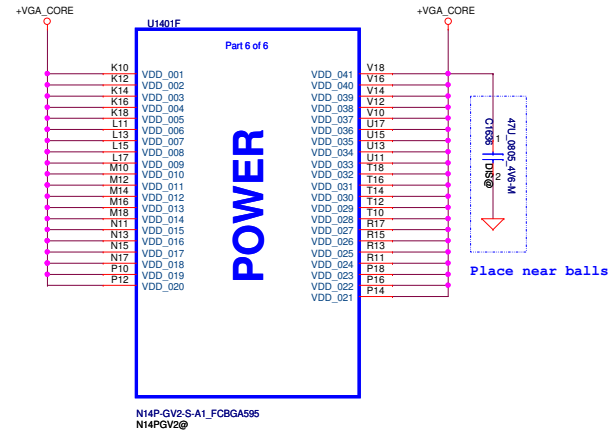
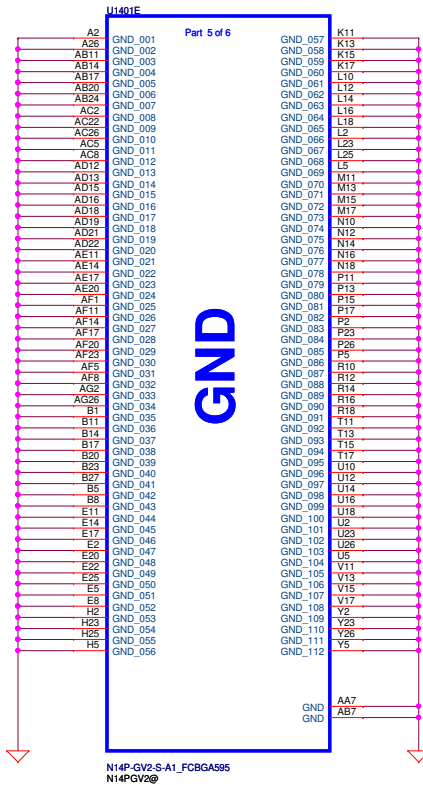
PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

(MB_ID=2)
(MB_ID=0)

www.teknisi-indonesia.com

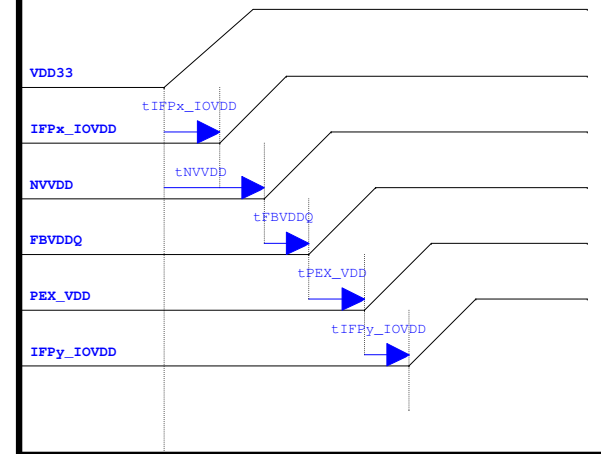






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VDD33 (+3VS_VGA)
IFPx_IOVDD
NVVDD (+VGA_CORE)
FBVDDQ (+1.5VS_VGA)
PEX_VDD (+1.05VS_VGA)



NV Recommended Power On Sequencing Order

X=A and B
Y=C, D, E and F

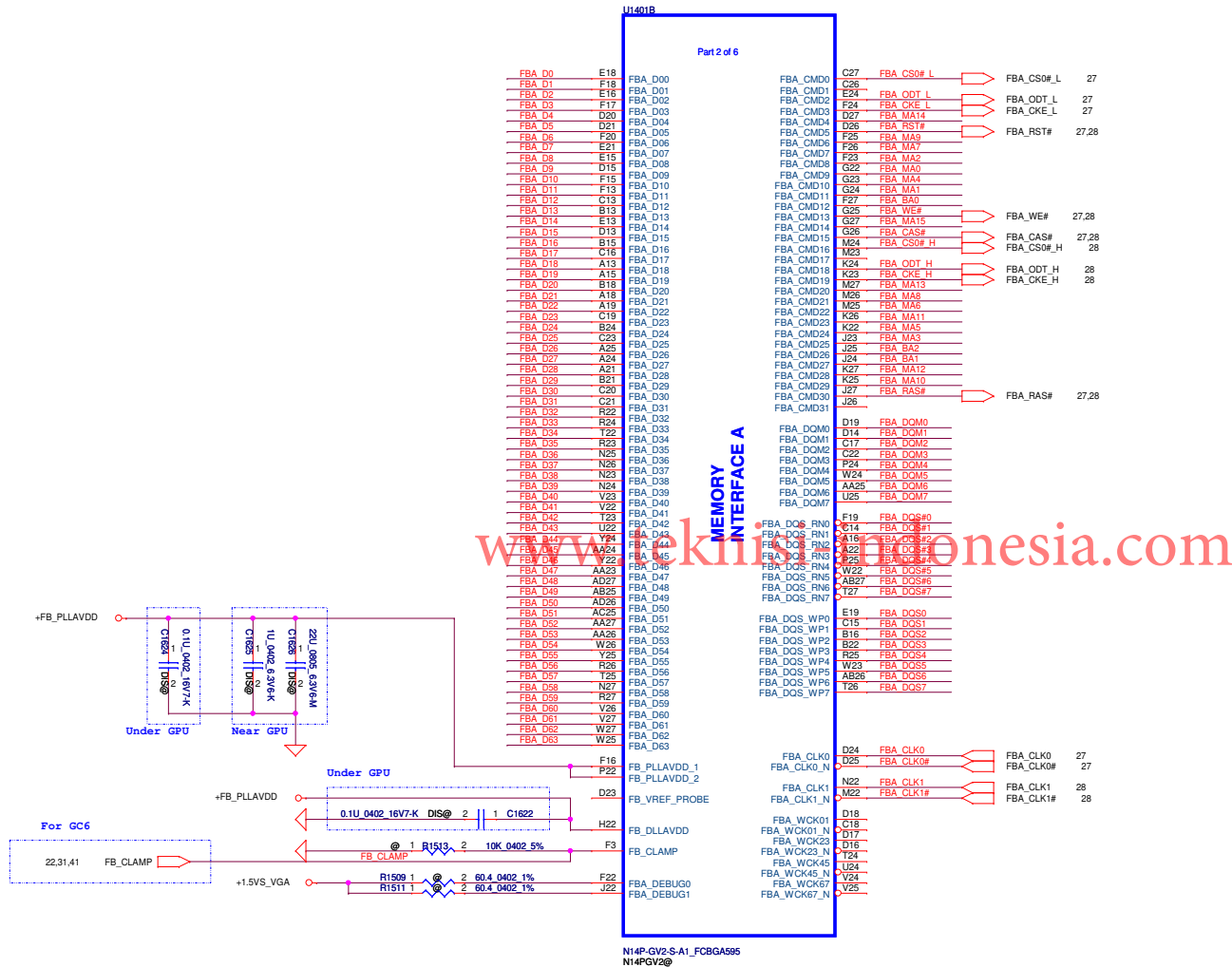
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	N14P_VGA CORE, GND	
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27,28 FBA_D[0..63] FBA_D[0..63]
27,28 FBA_DQM[7..0]
27,28 FBA_DQS[7..0]
27,28 FBA_DQS# [7..0]

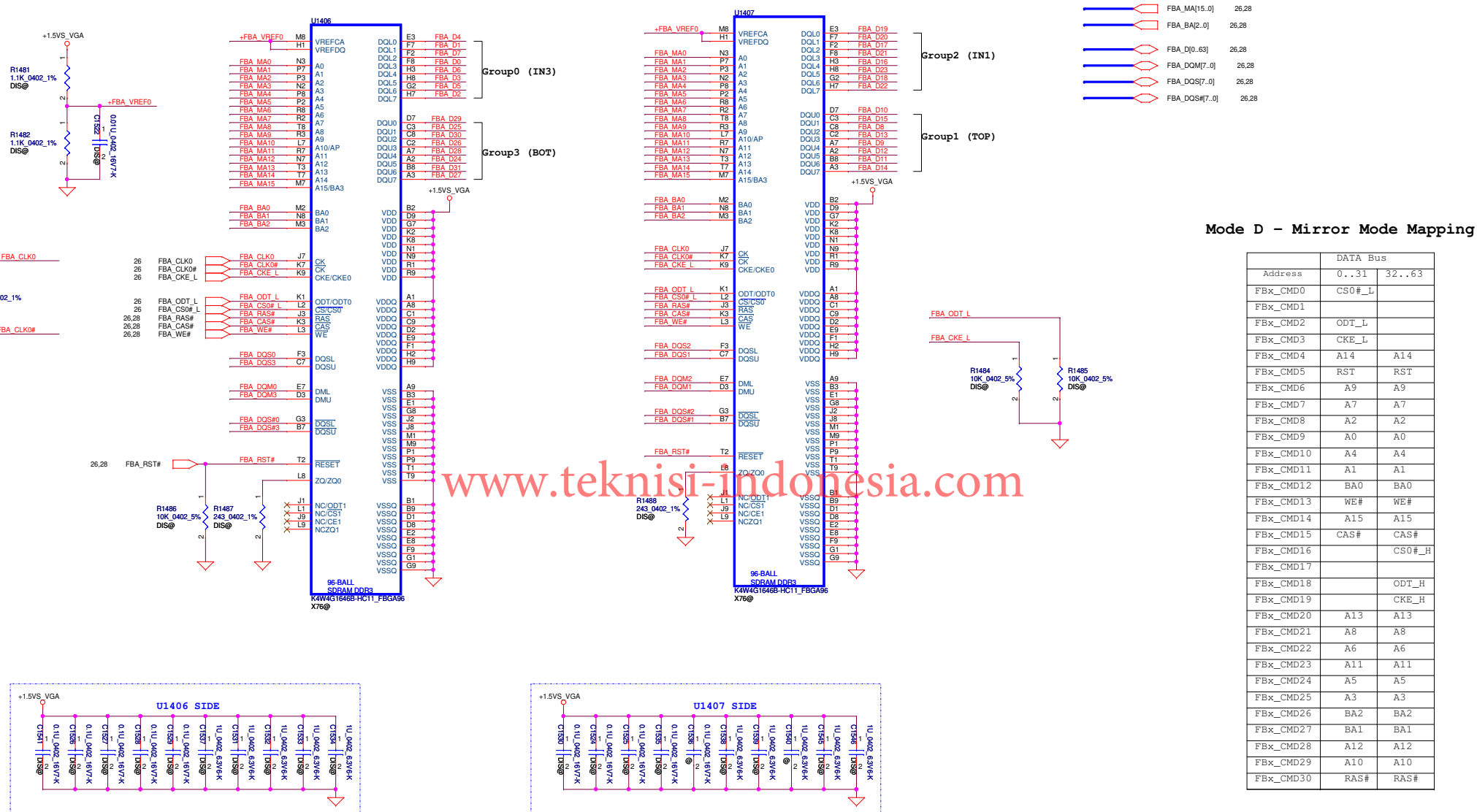
FBA_MA[15..0] 27,28
FBA_BA[2..0] 27,28

Mode D - Mirror Mode Mapping


Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



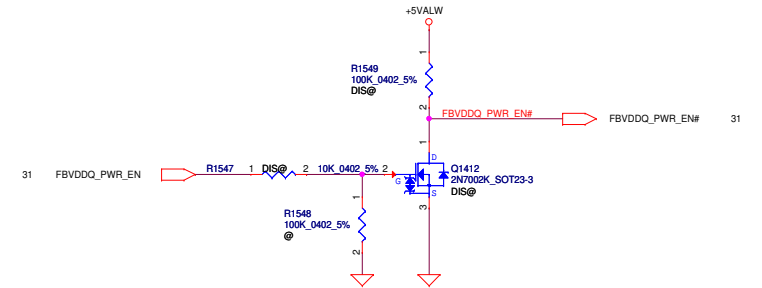
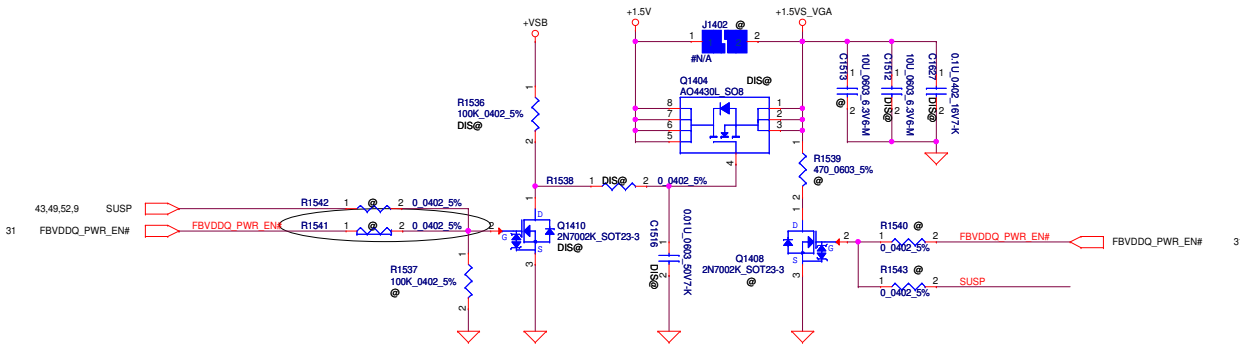
Memory Partition A - Lower 32 bits



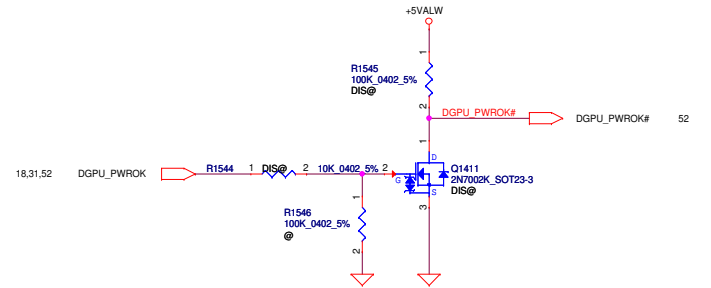
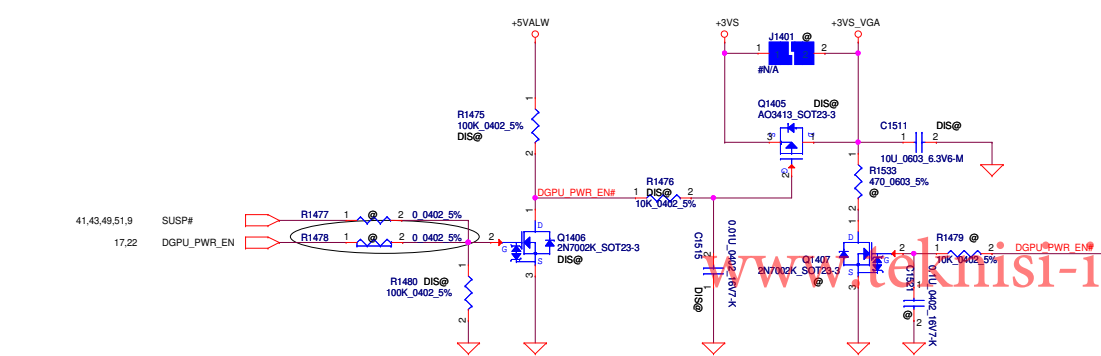
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						Custom	NM-A044	1.A				
Date:						Wednesday, February 06, 2013			Sheet	30	of	59

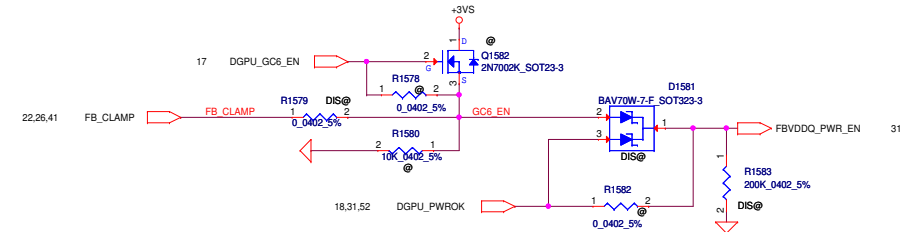
+1.5V to +1.5VS_VGA

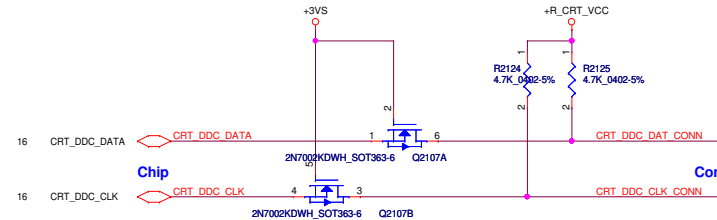
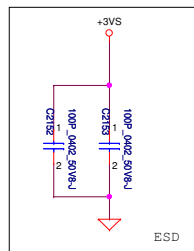
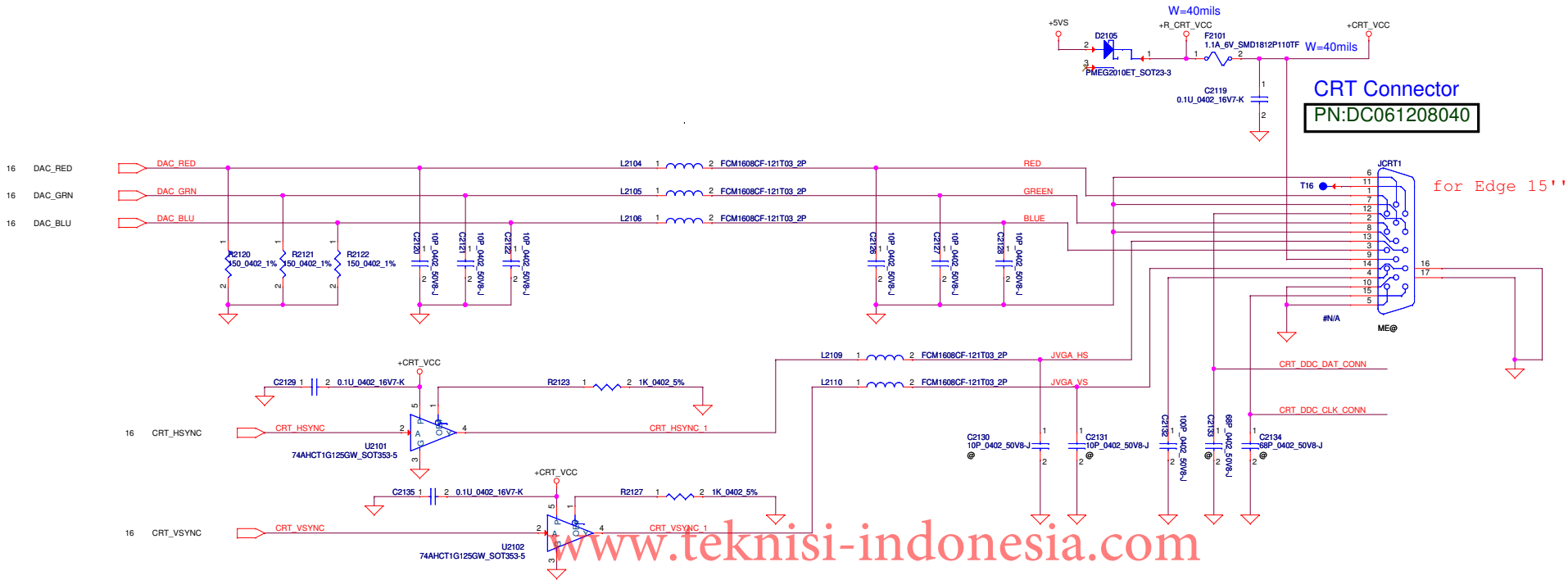



+3VS to +3VS_VGA

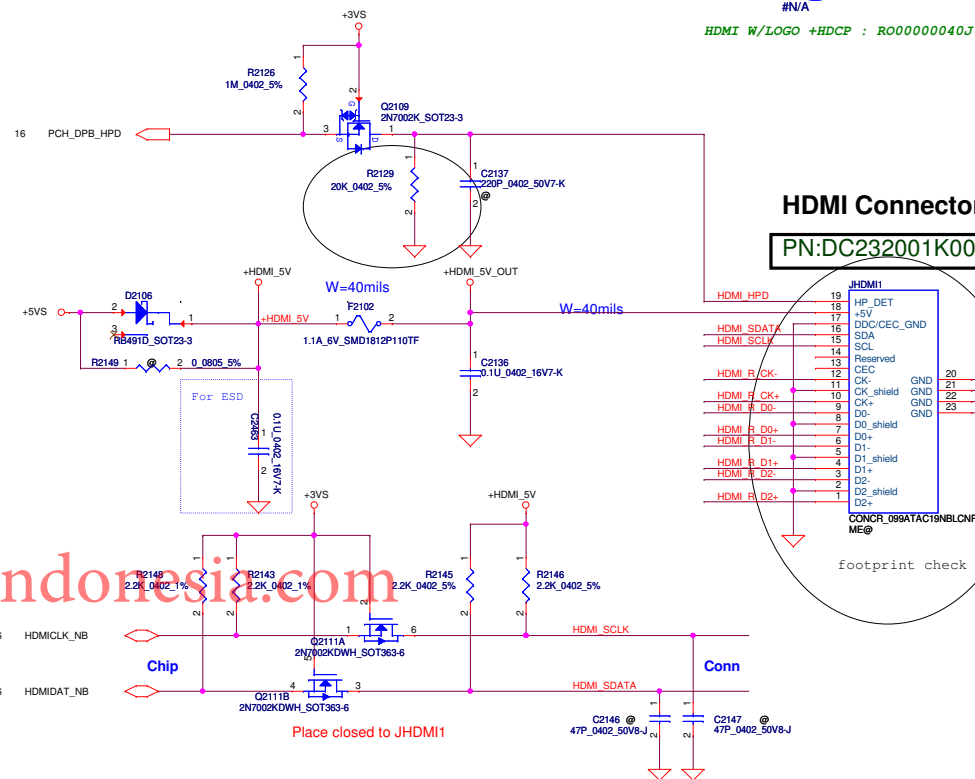
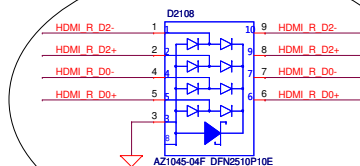
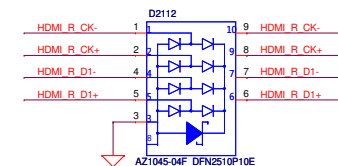
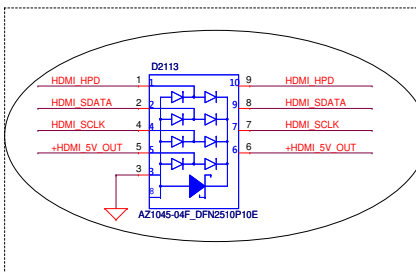
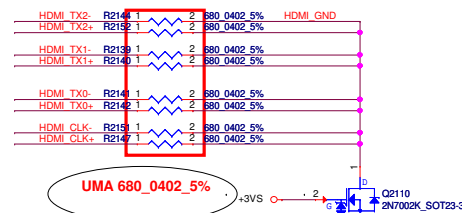
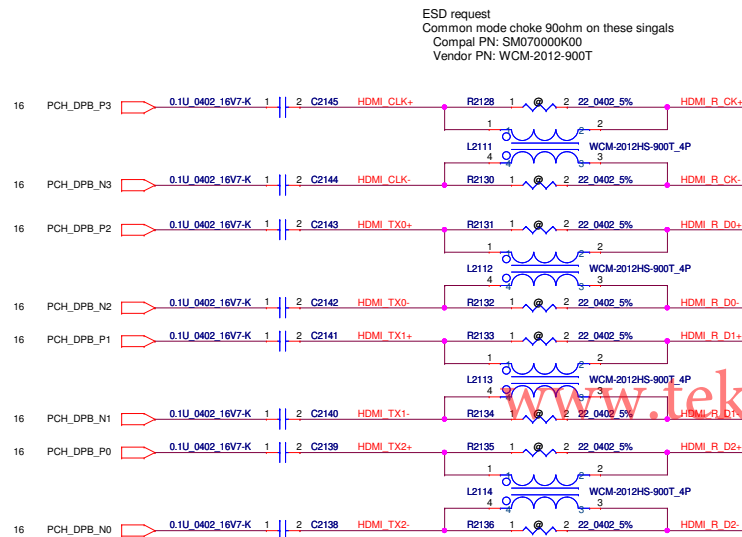


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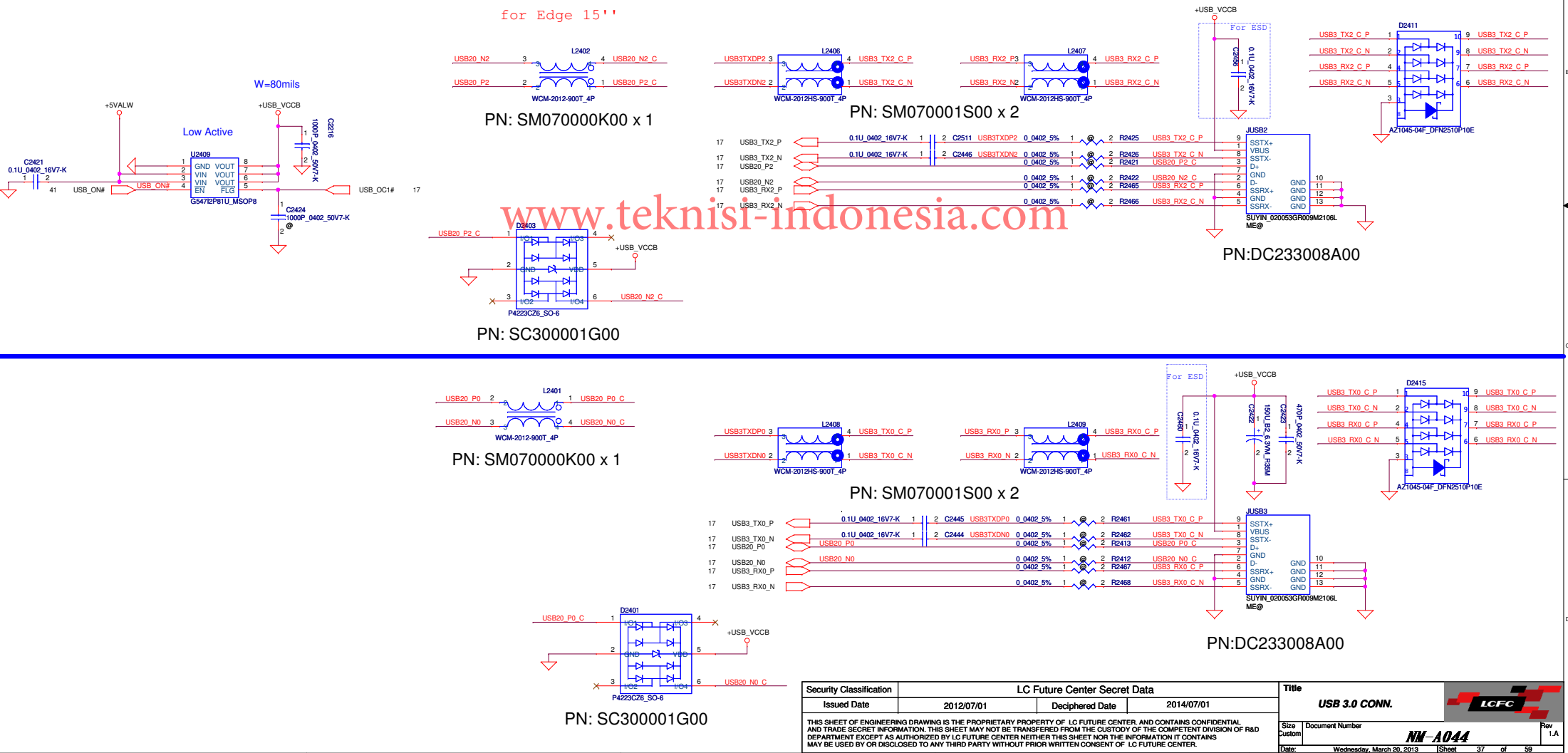




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Issued Date	2012/07/01	Deciphered Date	2014/07/01	CRT CONN.	
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				Size Custom	Document Number
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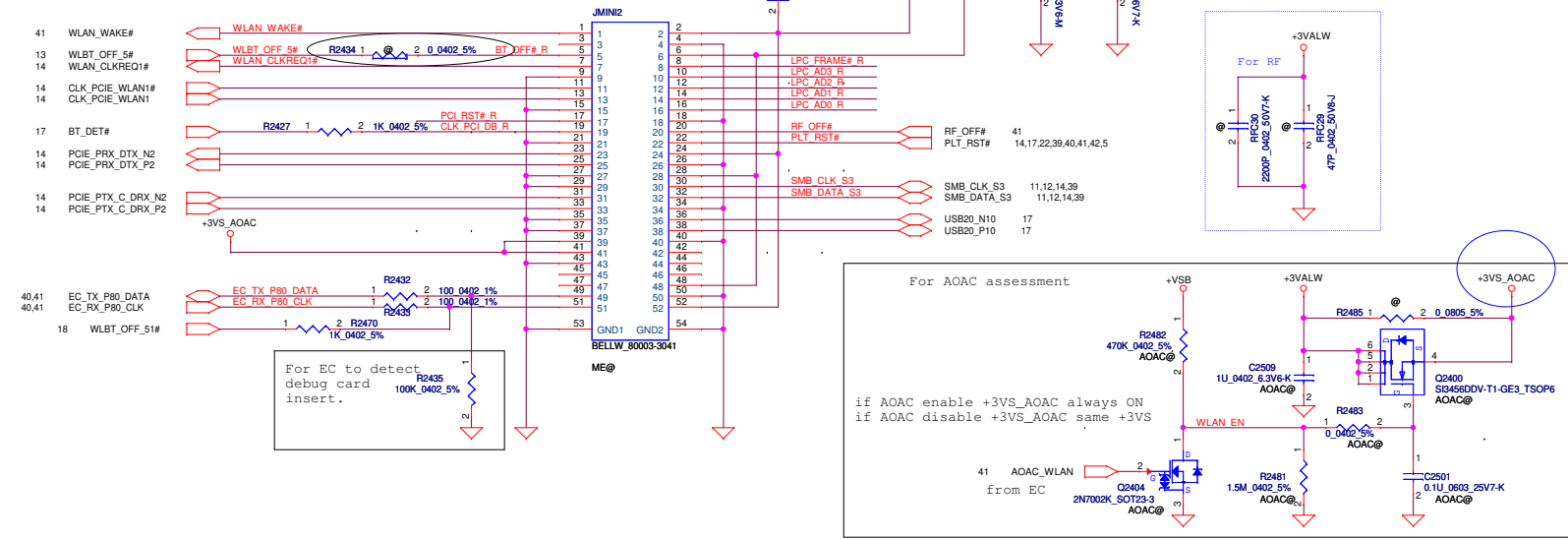
USB 3.0 Conn.



Mini-Express Card for WLAN(Half)

Mini-Express Card(WLAN)

PN:SP07000JP00



Mini Card Power Rating

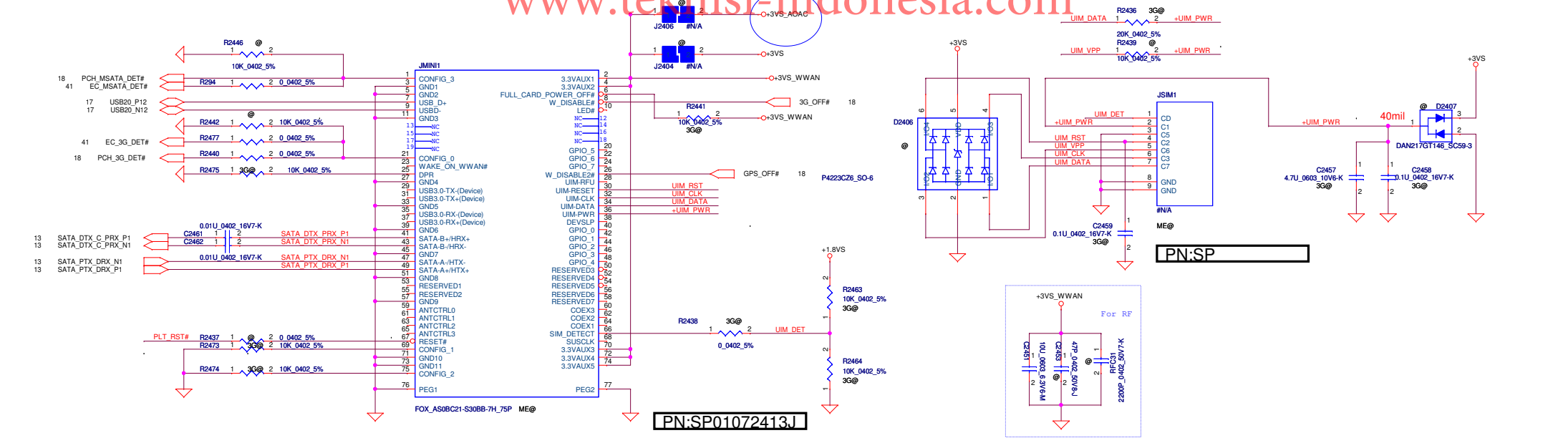
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

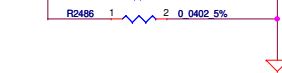
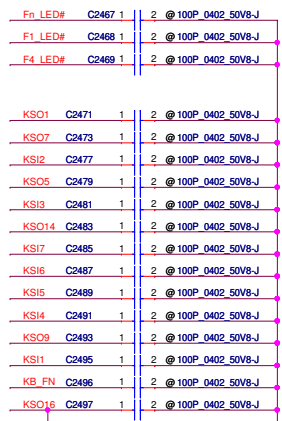
LPC_FRAME# R	R2449	1	2	0.0402 5%	LPC_FRAME#		LPC_FRAME#	13,40,41
LPC_AD3 R	R2455	1	2	0.0402 5%	LPC_AD3		LPC_AD3	13,40,41
LPC_AD2 R	R2456	1	2	0.0402 5%	LPC_AD2		LPC_AD2	13,40,41
LPC_AD1 R	R2457	1	2	0.0402 5%	LPC_AD1		LPC_AD1	13,40,41
LPC_AD0 R	R2458	1	2	0.0402 5%	LPC_AD0		LPC_AD0	13,40,41
PLT_RST# R	R2459	1	2	0.0402 5%	PLT_RST#		PLT_RST#	13,40,41
CLK_PCI_DB R	R2428	1	2	0.0402 5%	CLK_PCI_DB		CLK_PCI_DB	17,40

Mini-Express Card for WWAN/mSATA(Full)

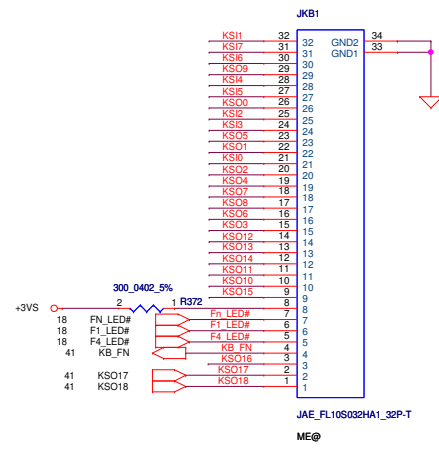
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INT_KBD Conn.

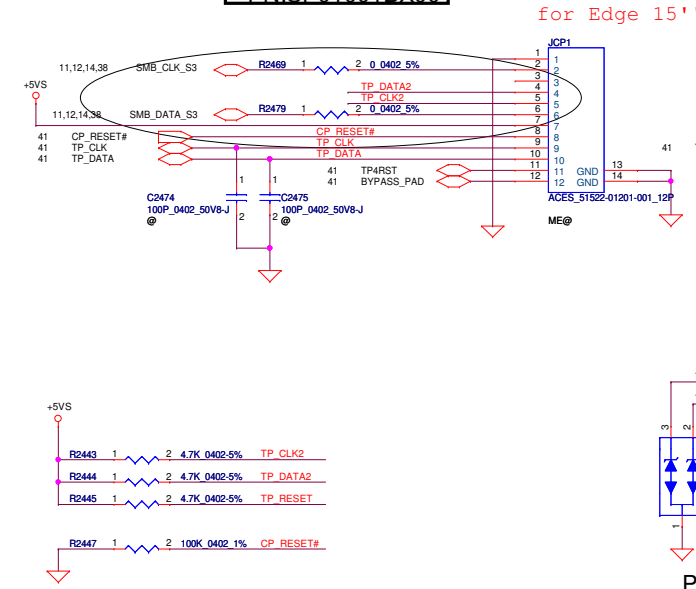


PN:SP011208010



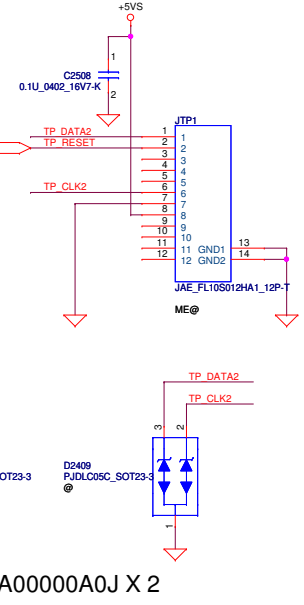
Click pad

PN:SP01001BX00



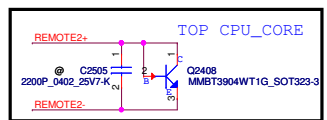
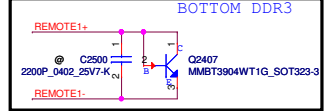
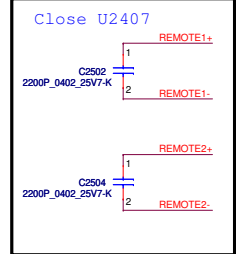
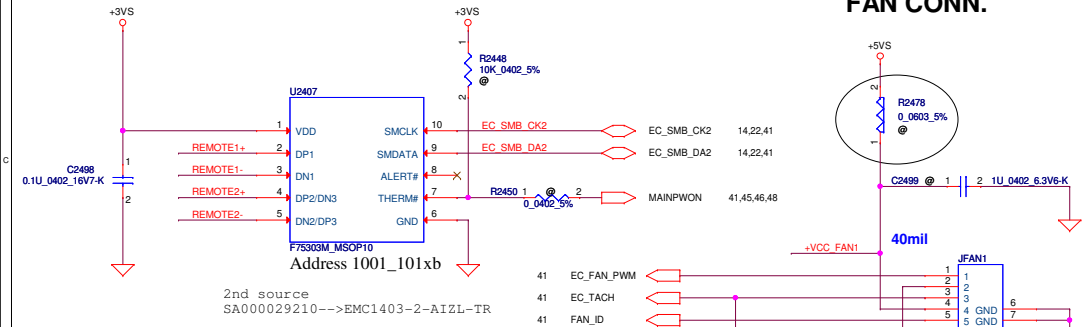
Track point

PN:SP01120802J



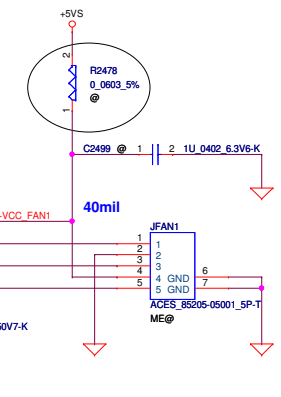
PN: SCA00000A0J X 2

Fintek thermal sensor placed near by TOP DDR3



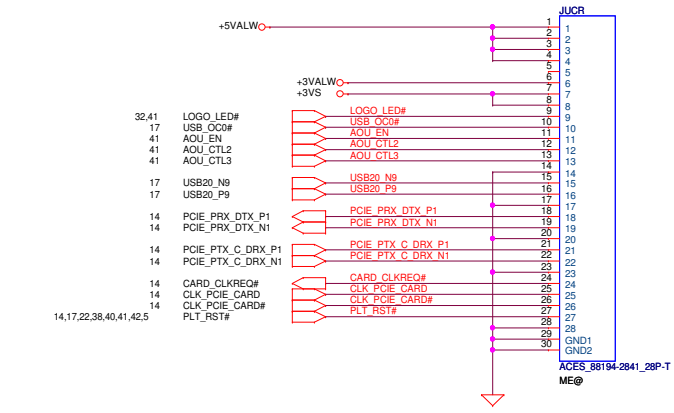
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN CONN.



PN:SP02000U900

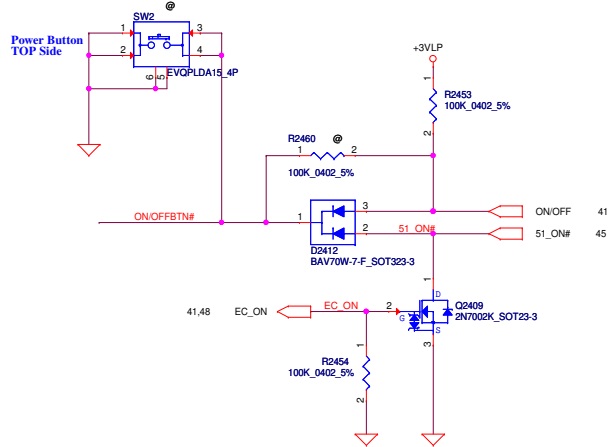
Audio+CF Board



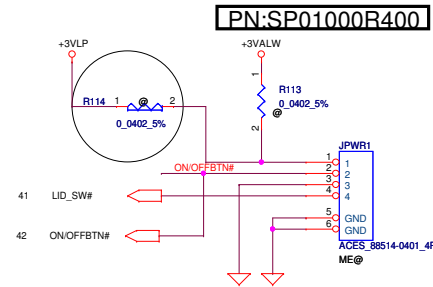
Security Classification				LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01			KB/TP/Thermal Sensor/Audio	
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				Date	Wednesday, March 20, 2013	Sheet	39 of 59

ON/OFF switch

Power Button



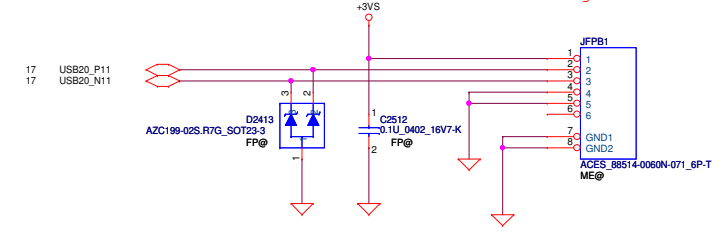
Power Button CONN.



Finger Print Board

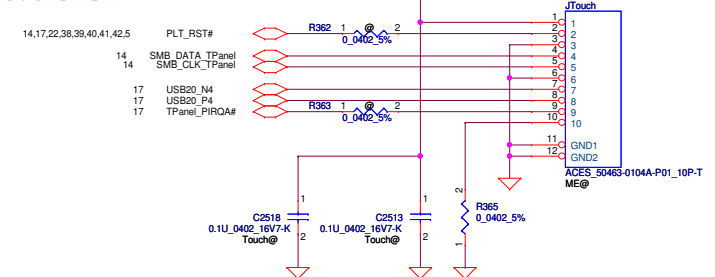
PN:SP01000R400

for Edge 15''



Touch Panel

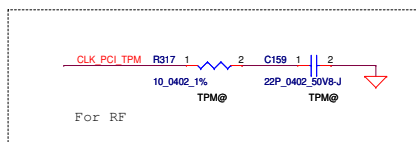
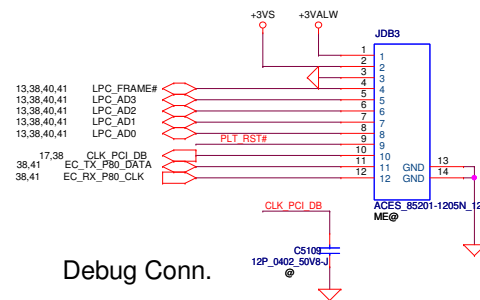
for Edge 15''



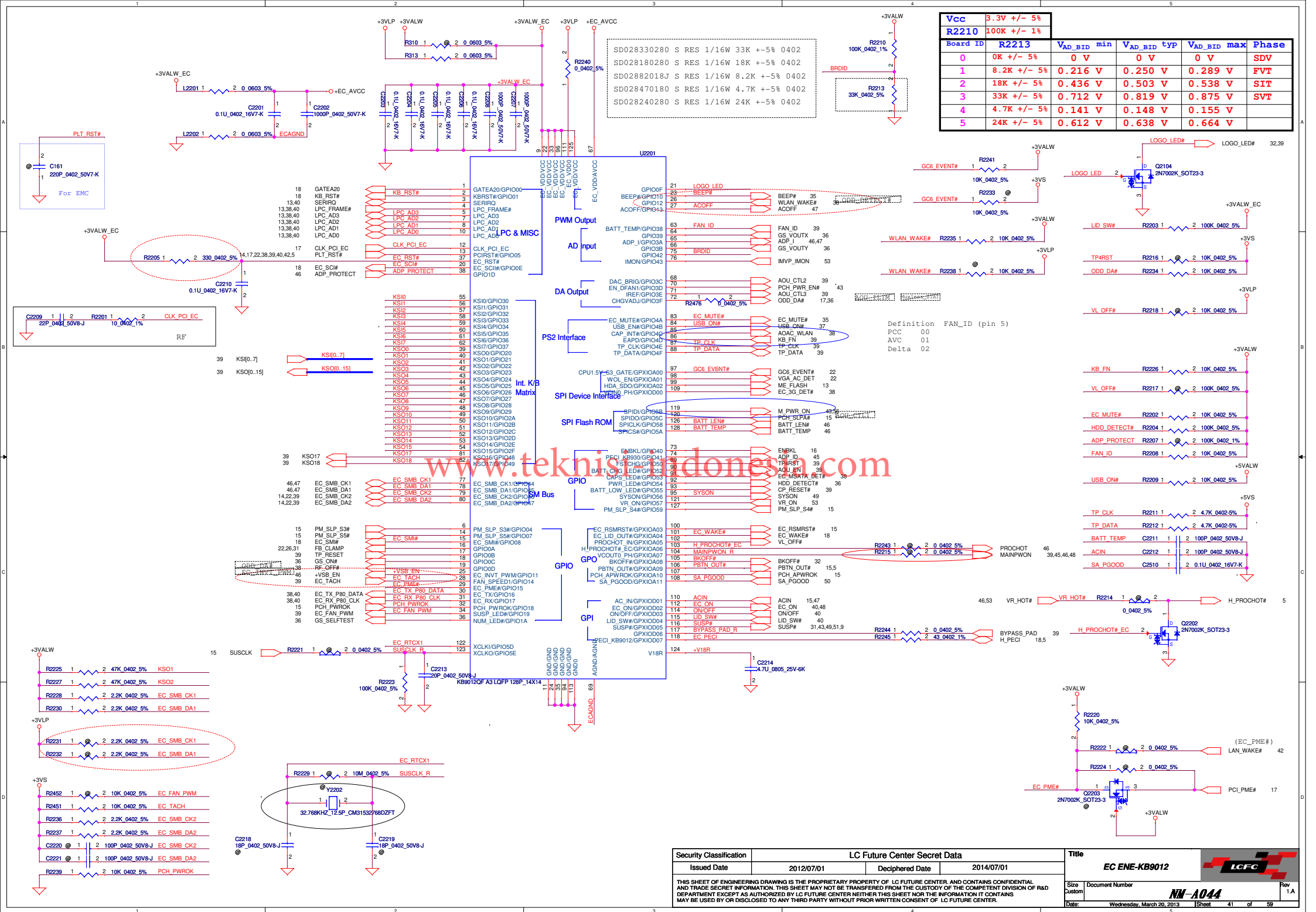
TPM

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Debug Conn.

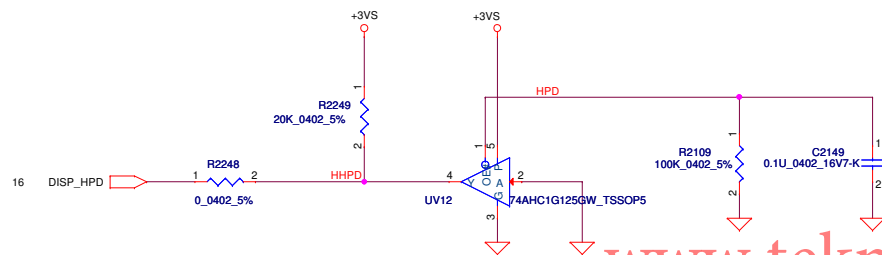


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				Date		Wednesday, March 20, 2013	Sheet 40 of 59

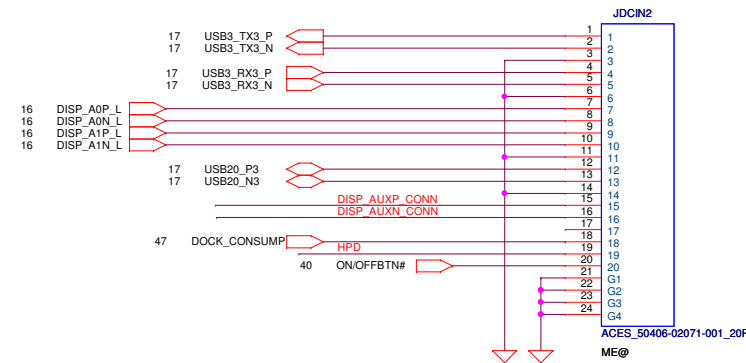
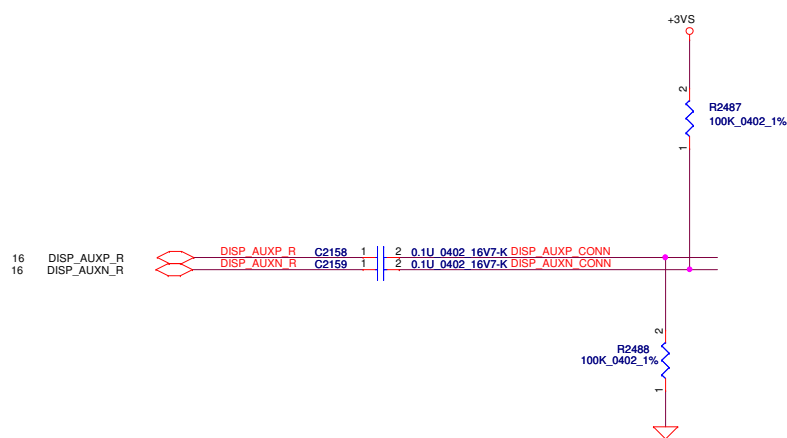


Vcc		3.3V +/- 5%			
R2210		100K +/- 1%			
Board ID	R2213	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

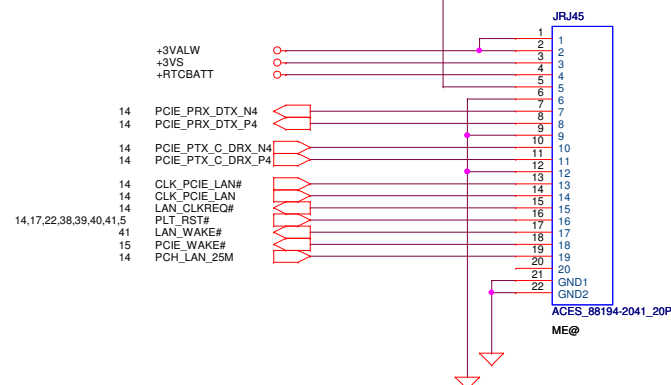
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2012/07/01		2014/07/01		Rev	
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A		NM-A044		1.A	
Date		Wednesday, March 20, 2013		Sheet	
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		59			



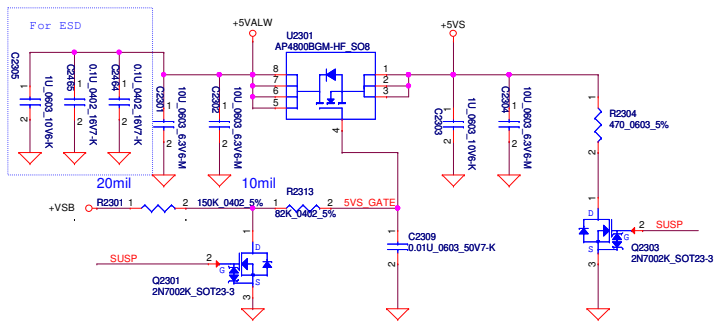
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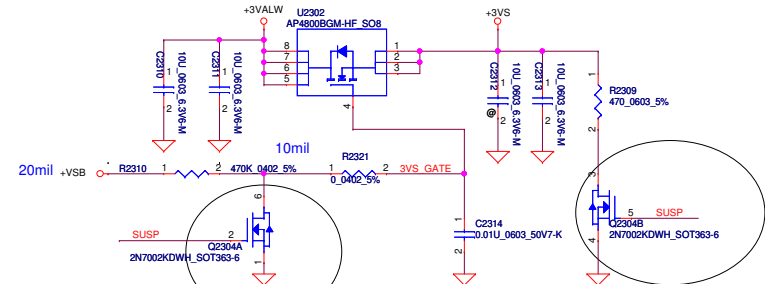
RJ45 Board



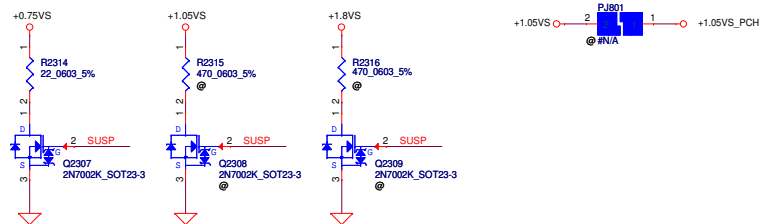
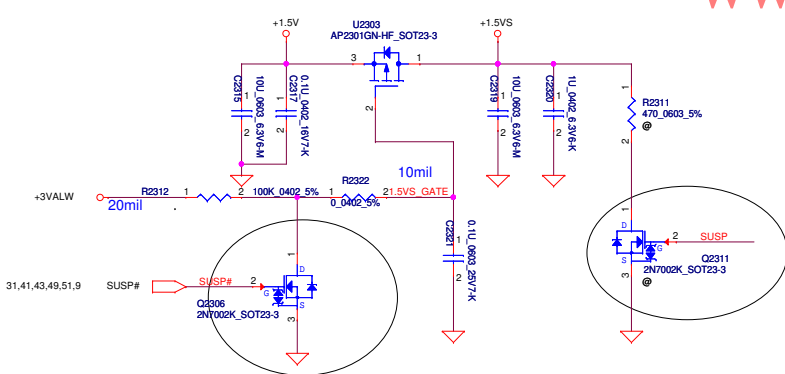
+5VALW TO +5VS



+3VALW TO +3VS

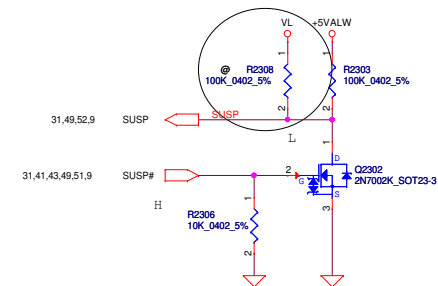
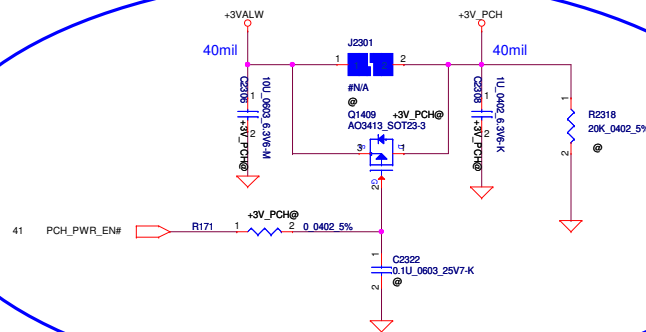


+1.5V to +1.5VS

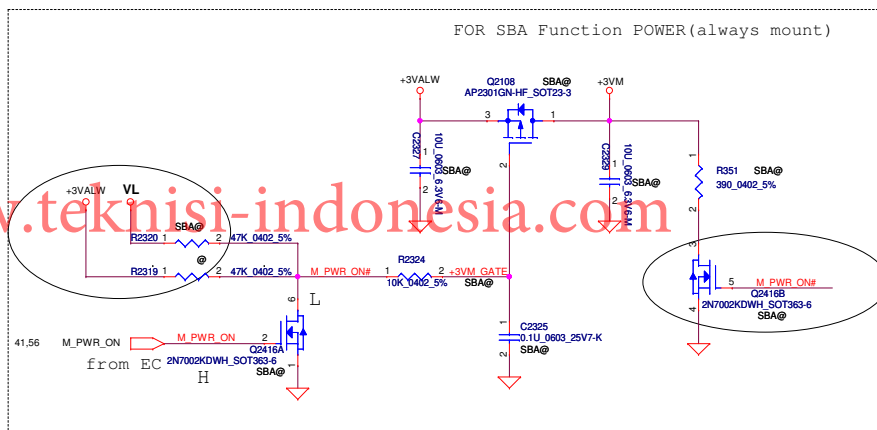



+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3

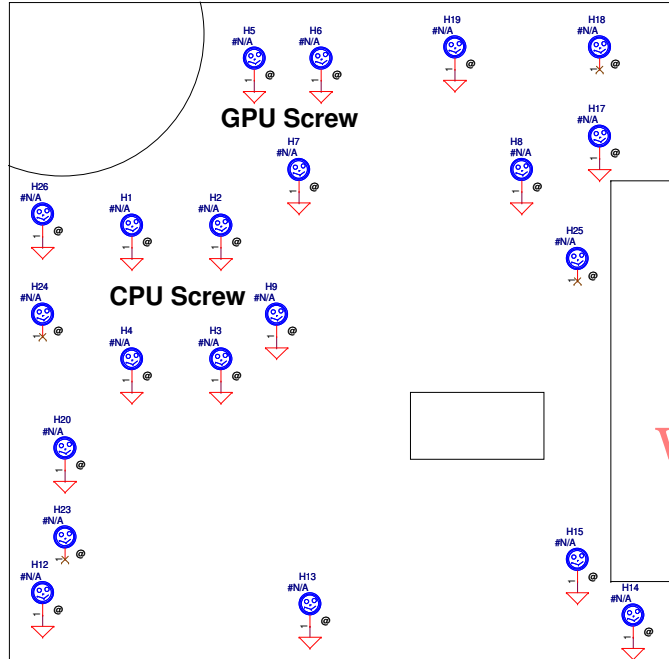


FOR SBA Function POWER(always mount)



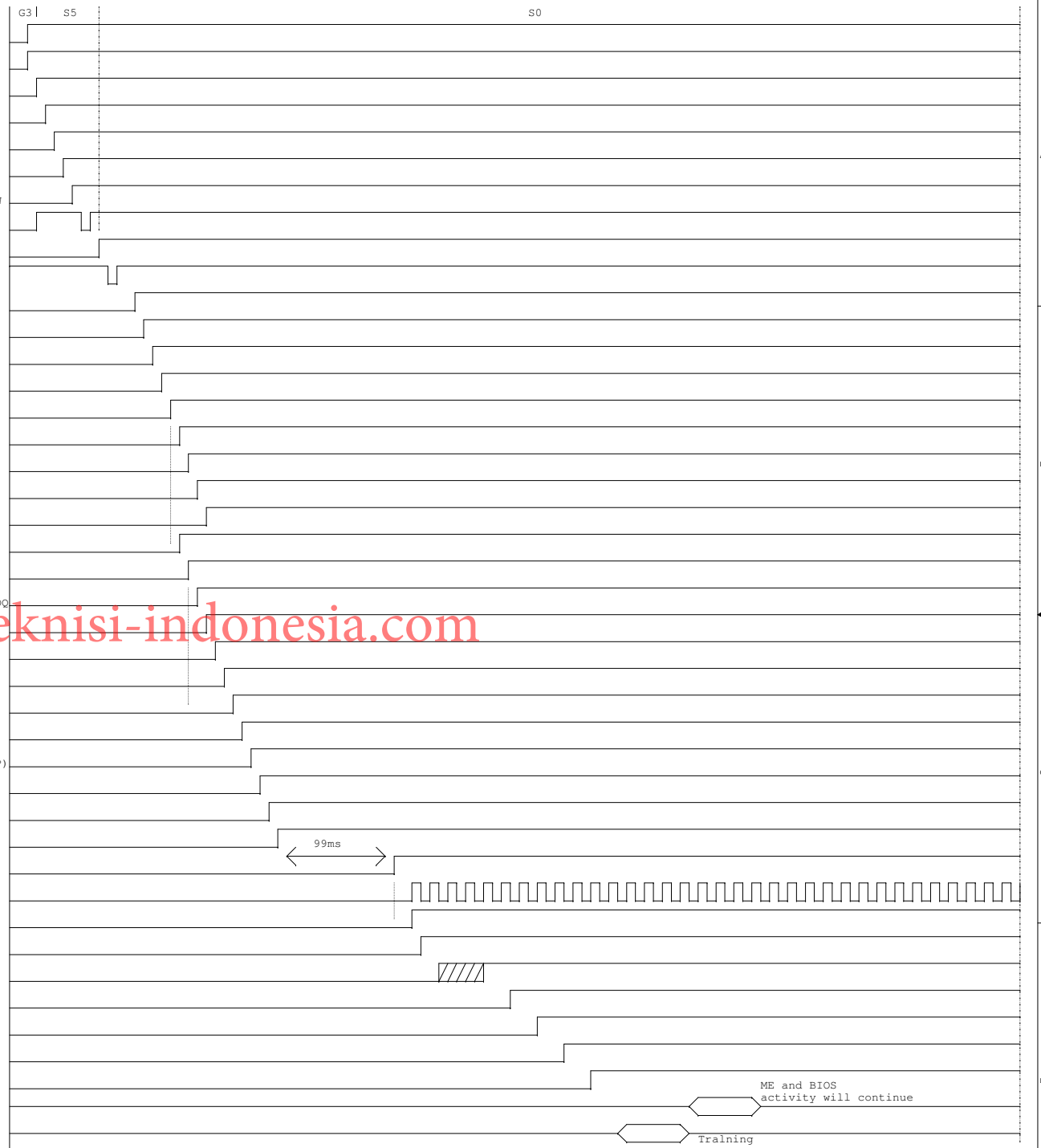
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Issued Date		2012/07/01		Deciphered Date		2014/07/01				
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Screw Hole & FD



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RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
PCH_SLPA#
M_PWR_ON
+3VM
+1.05VM
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI



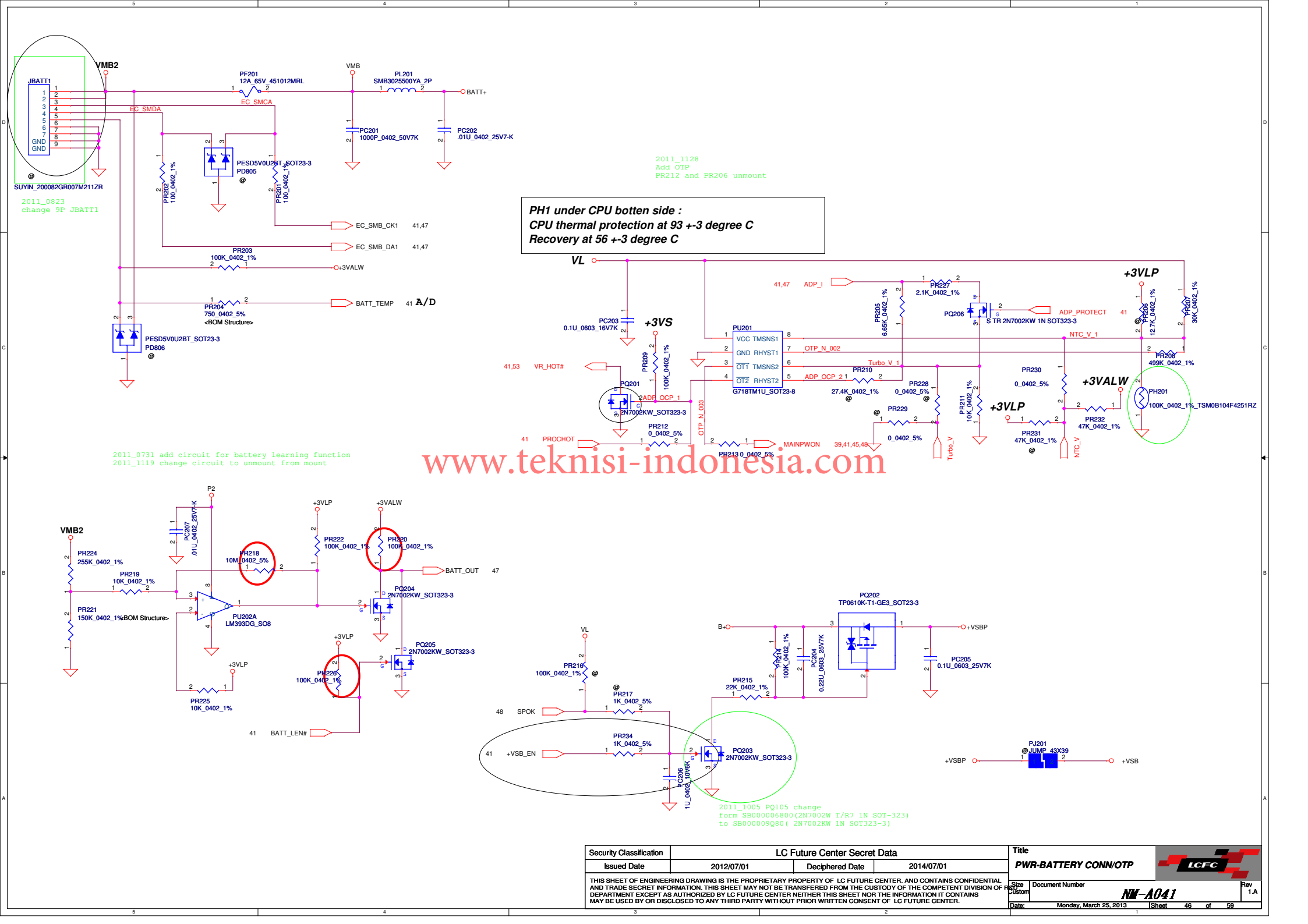
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				Date:	Wednesday, March 20, 2013
				Sheet	44 of 59

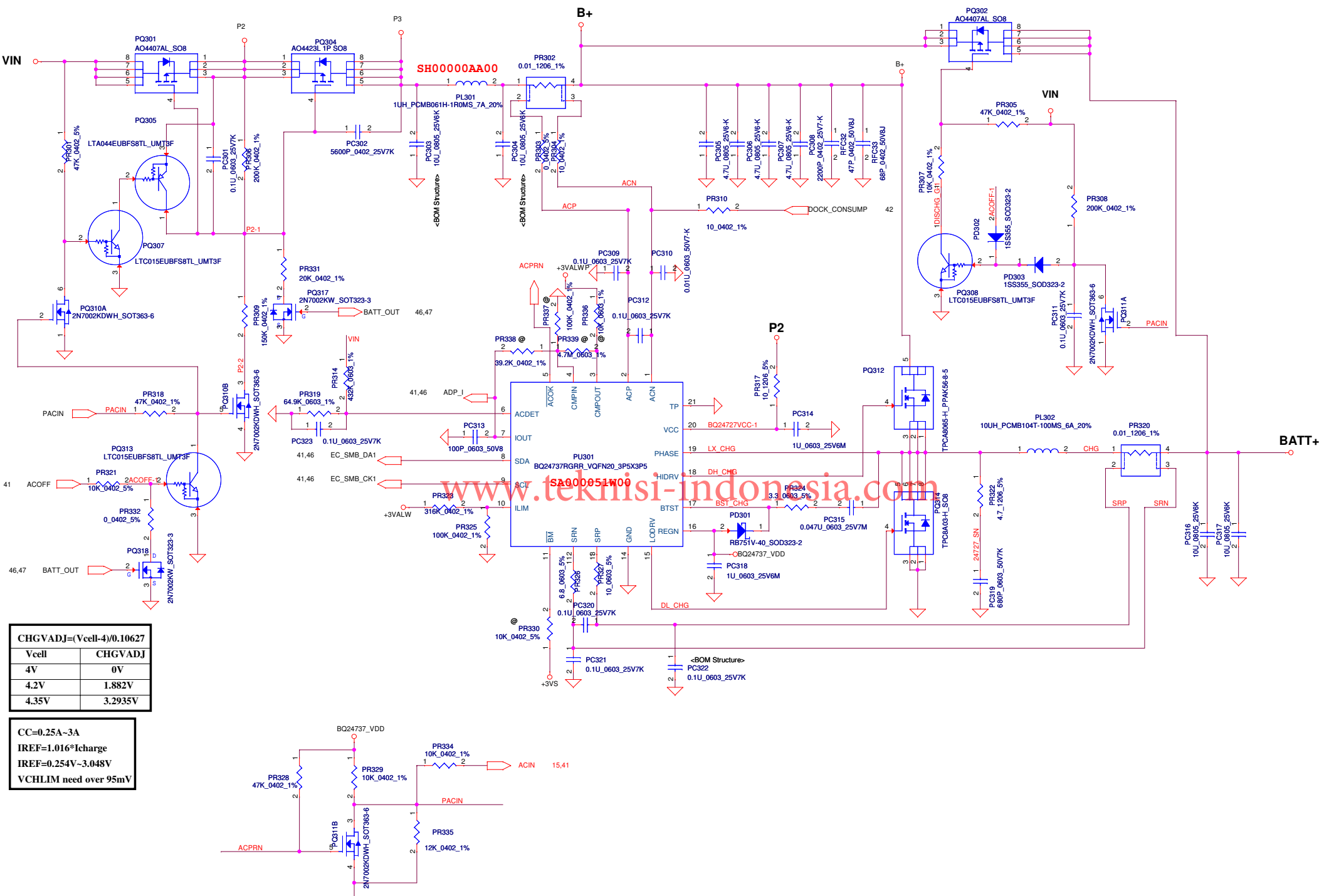
ME and BIOS activity will continue

Training



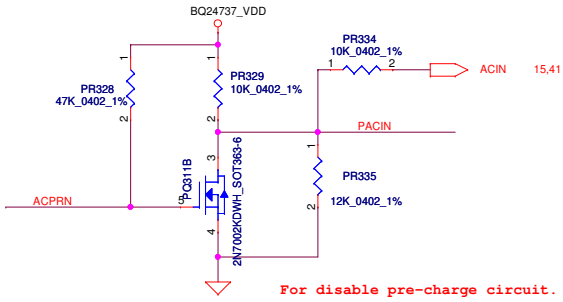
Rev 1.A

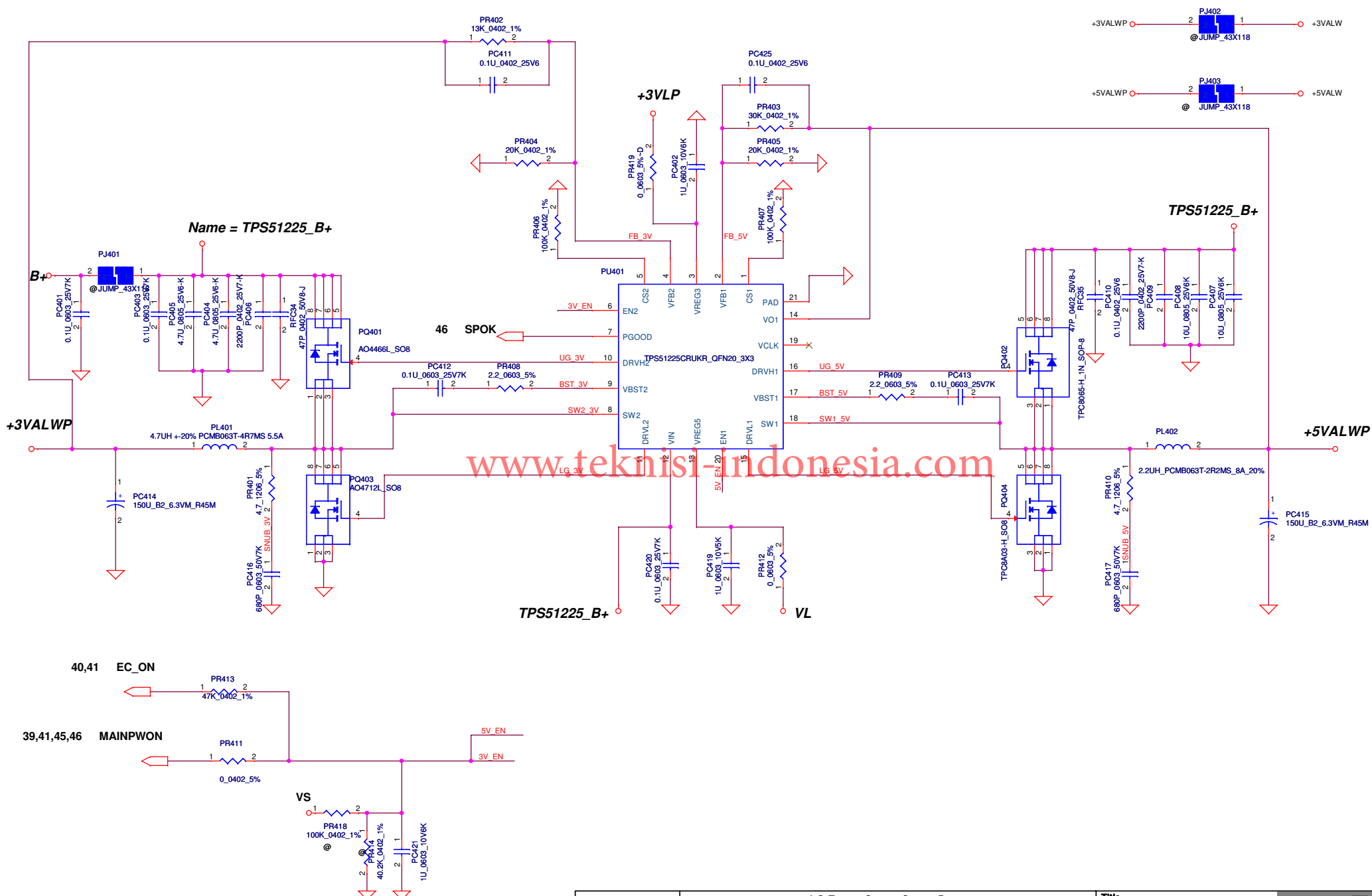




CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

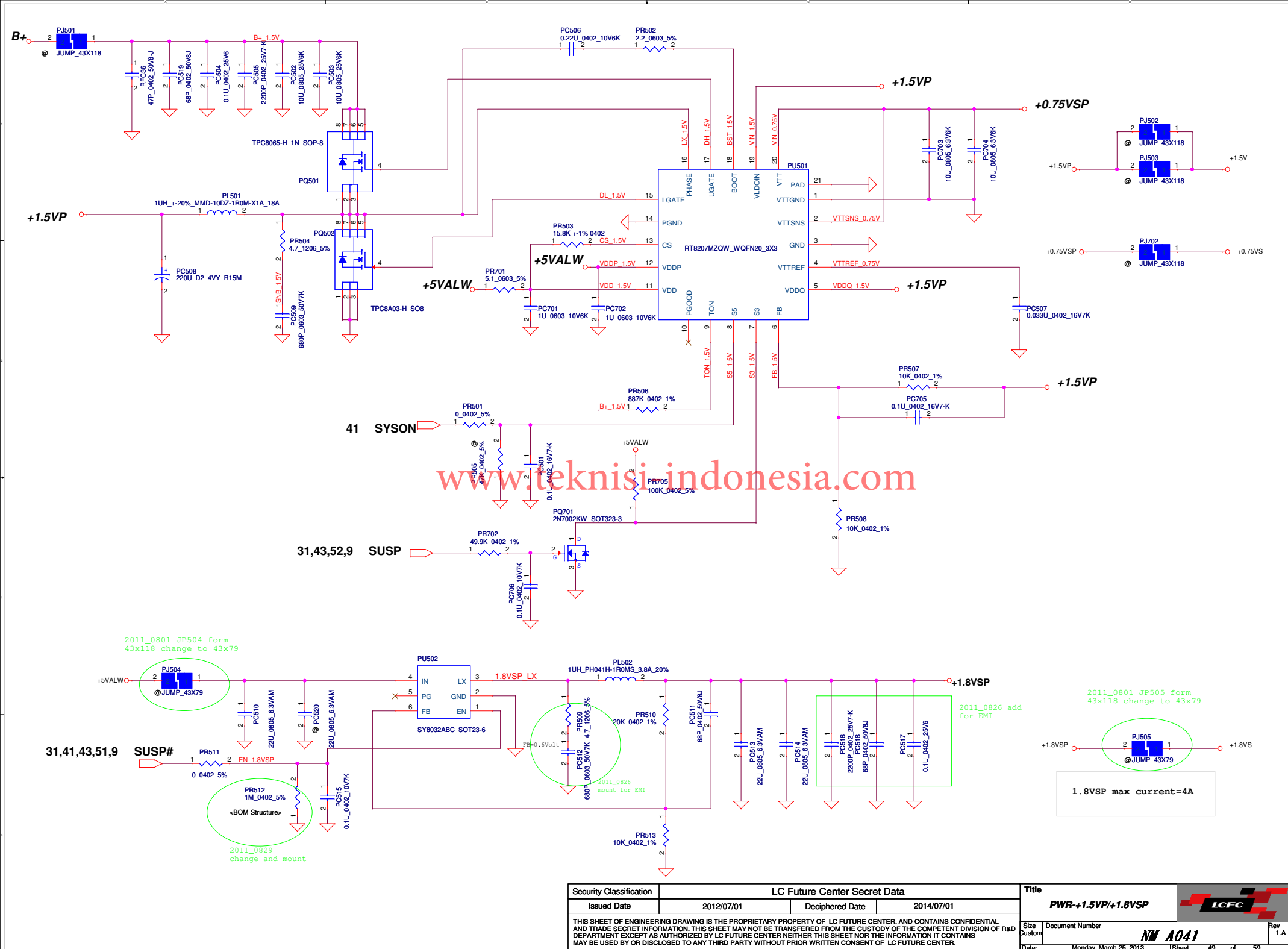


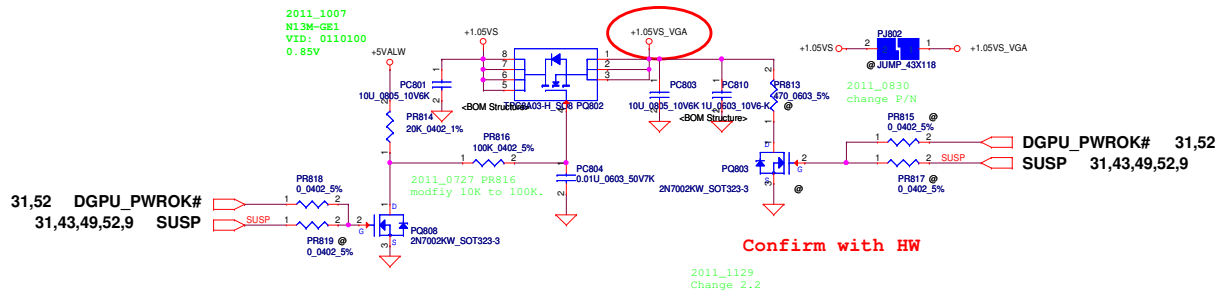
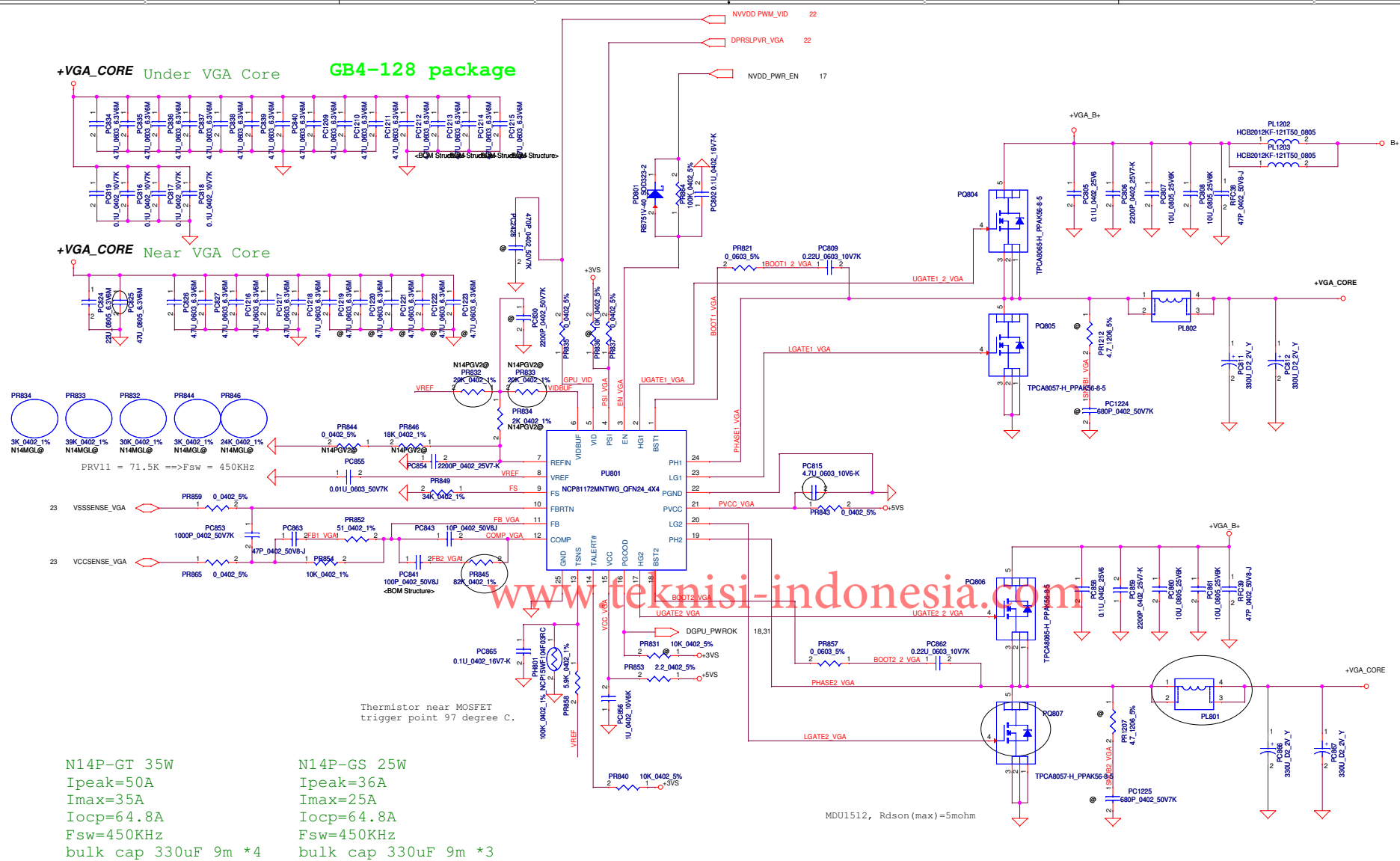


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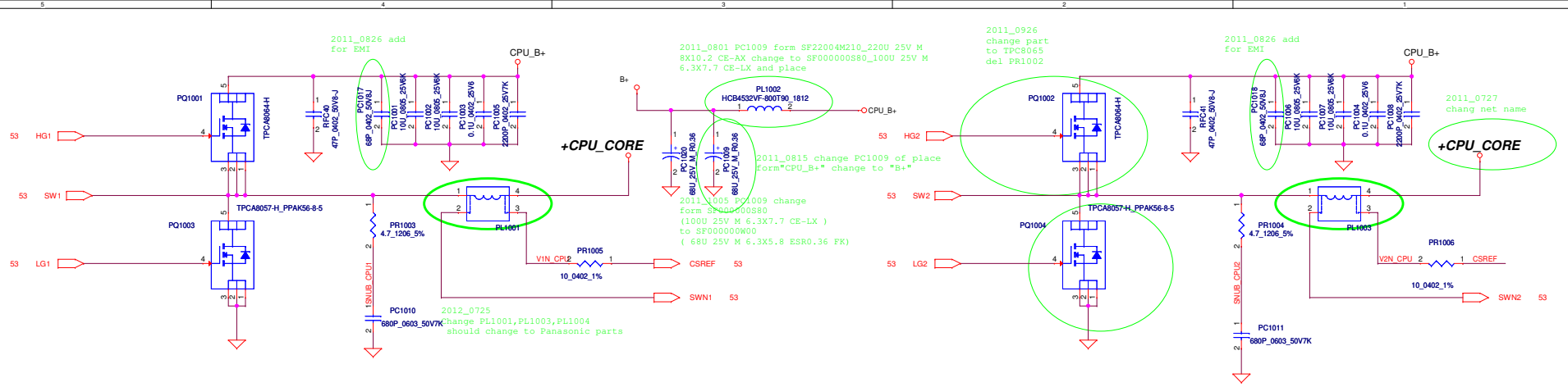
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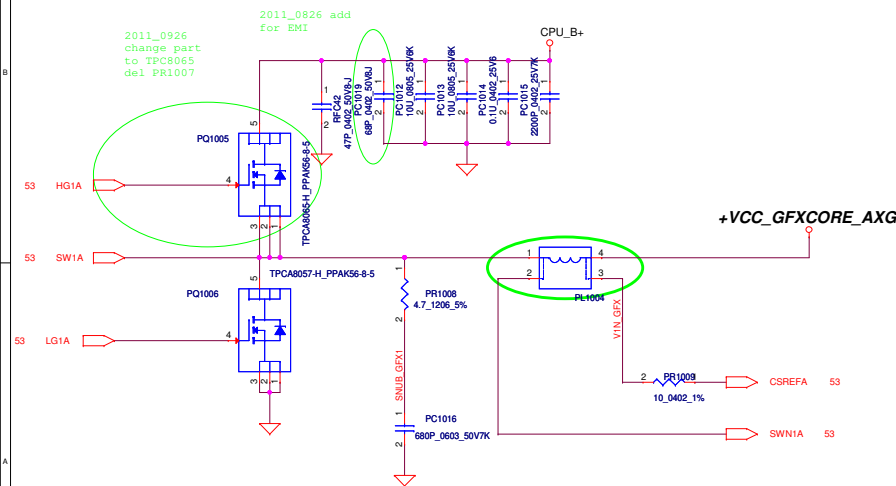




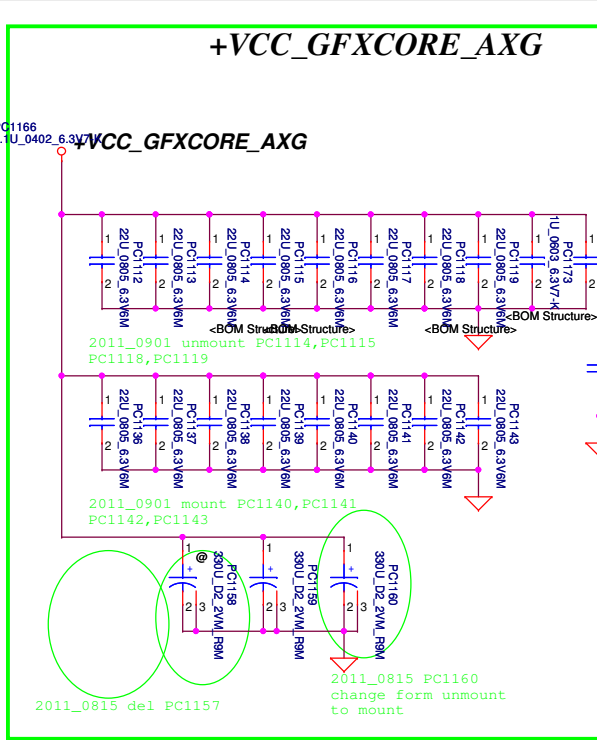
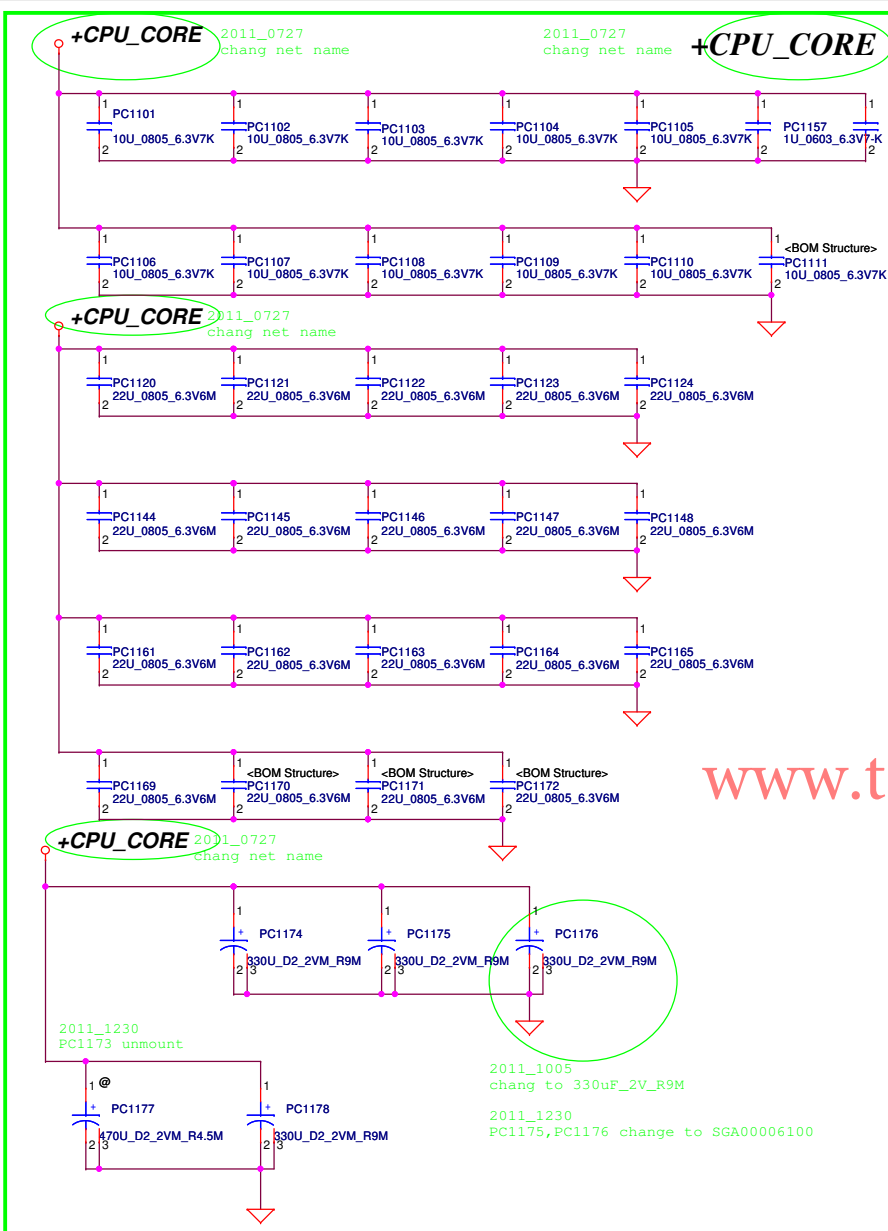
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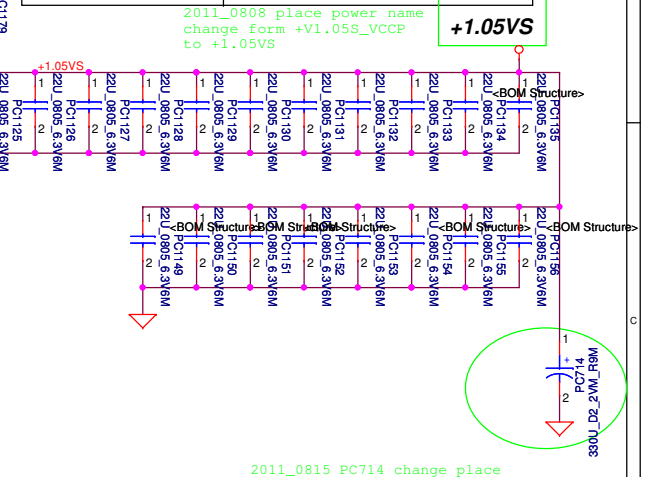


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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



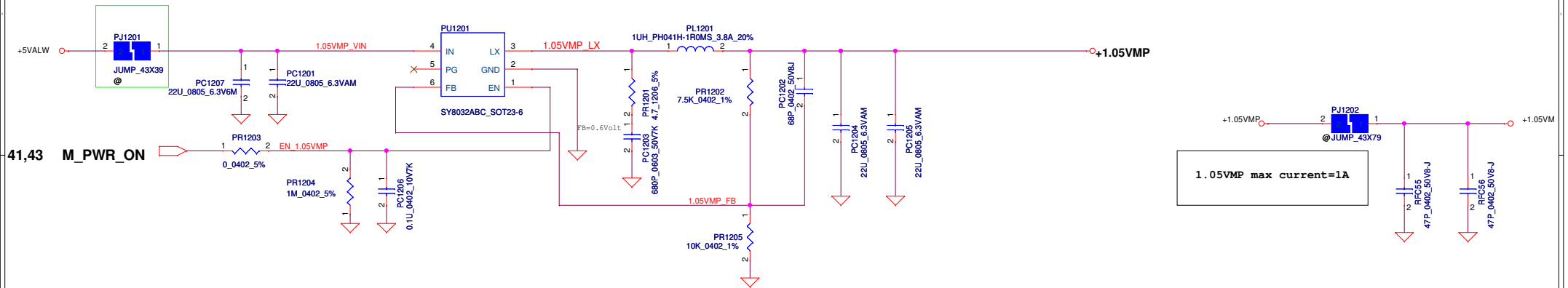
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2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to 330uF_2V_R9M

2011_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U_D2_2.5VY_R9M)


2011_0923 JUMP form 43X79 change to 43X79



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2012/09/XX	No1	V	V	V	Add CXXX, CXXX	Add XXX function

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